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A 390 dpi Live Fingerprint Imager Based on Feedback Capacitive Sensing Scheme

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Abstract

A single-chip 200×200*-element sensor array for fingerprint acquisition is presented. The sensor produces a gray-scale image linearly related to the depth of the ridges. The fingerprint is captured at* 10 *Frames/s by pressing the finger skin onto the chip surface. The area of the sensor is* $15 \times 15mm^2$ *and its power consumption is below* $600\mu W$.

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This paper introduces a single-chip, 200×200-element sensor array which is able to grab the fingerprint pattern without any use of optical and mechanical adaptors. Using this integrated sensor the fingerprint is captured at a rate of 10 F/s by pressing the finger skin onto the chip surface. The fingerprint pattern is sampled by capacitive sensors which detects the electric field variation induced by the skin surface. The entire architecture is integrated in a standard 2-metal digital CMOS technology.

The idea of using a capacitive sensor array for detecting fingerprints has been already described in [1,2] but no implementation, to our knowledge, has been so far documented. The sensor described here uses a substantially different scheme from the previous approaches which is based on feedback capacitance sensing principle as depicted in Fig. 1 where the cross-section of two cells is shown. Two metal-2 plates are adjacently placed in the cell area and separated from the skin surface by the passivation oxide. The skin surface can be thought of as a third plate opposed to the metal-2 ones and separated by a dielectric layer with variable thickness composed of air. This structure realizes, by a lumped-model point of view, a two series-connected capacitors scheme. The metal-2 plates are separately connected to the input and output of an high-gain inverter, thus realizing a charge integrator. The cell works in two phases: first, the charge amplifier is reset shorting the input and output of the inverter. During this phase, the output of the inverter settles to its logical threshold V_t. During the second phase, a fixed amount of charge δQ is sinked from the input causing an output voltage swing inversely proportional to the feedback capacitance value. Since the feedback capacitance is inversely proportional to the distance of the skin, a linear dependence of the output voltage versus the skin distance is expected. In other words, for a fixed amount of sinked charge, the output voltage of the inverter will range between two extrema depending on the feedback capacitance value: i) the upper saturation level if no feedback capacitance is present; ii) a value close to the logical threshold when the feedback capacitance is large.

Even if a linear response is expected, the inverter gain and the parasitic capacitance of the input play a role reducing the linearity of the characteristic. In fact, for a limited gain A of the amplifier the output swing is given by:

$$\Delta V_o = -\delta Q \ / \ \left[\frac{C_l}{A} + (1 + \frac{1}{A}) C_r \right],$$

where C_r is the sensed feedback capacitance, composed of the sum of a fixed parasitic capacitance and a variable one which has to be sensed, and C_l is the parasitic input capacitance, as illustrated in Fig. 1. The simulated behavior of the cell is plotted in Fig. 2. The solid line curve represents the estimated feedback capacitance value versus skin distance for a typical $0.7\mu m$ CMOS process and designed cell dimensions. The dashed line represents the cell behavior for an infinite gain inverter when parasitic capacitances are neglected, the dotted line is related to the theoretical behavior for an inverter gain equal to 3500, and $0.1 fF$ of fixed feedback parasitic capacitance and the cross-dotted line belongs to the layout-extracted cell schematic. Since distance between the skin and sensor surface identifies the presence of ridges and valleys, an array of cells is used to sample the fingerprint pattern.

A block diagram of the sensor is shown in Fig. 3. An array of cells is addressed in a raster mode by means of horizontal and vertical scanners. The chip also contains the timing control and voltage references. A more detailed schematic of the cell is illustrated in Fig. 4. Two transistors of the high gain cascode inverter M_2 and M_3 are used for addressing purposes, thus limiting the power consumption of the non-addressed cells. The output of the inverter is buffered by a source follower stage M_5 into a vertical output line by means of M_6. Transistor M_7, which is addressed by the horizontal shift register, greatly reduces the output capacitance of the follower stage since only one vertical line is shorted to the global output. Two plates of a very small capacitance C_i are connected to the input and to a node common to the whole array, respectively. When a negative voltage step ΔV_i is applied to the global node, a charge amount $\delta Q = C_i \Delta V_i$ is sinked from the amplifier input as previously explained. This mode of operation is very useful since the sensor can easily deal with different ranges of sensed capacitances by changing the amount of ΔV_i.

Great care has been devoted to the turning-off phase of the reset transistor M_8, since charge injection in the input node may saturate the amplifier. Anyway, it can be demonstrated that if the switch-off transient of the reset transistor is slow enough compared to the inverse of the gain-bandwidth product of the inverter, most of the channel charge of the reset transistor is injected into the output node. Additionally, the size of the switch transistor has to be kept small to reduce the absolute amount of injected charge. However, reducing the dimension of the switch transistor degrades the stability of the amplifier since reduces the loop gain bandwidth. In our design, we introduced a second stronger switching transistor M_9, activated at different phase than M_8. During the reset phase both transistors are set, reducing the resistance of the feedback loop, so that the output ringing is contained. During the charge integration phase, M_9 is first opened so that its channel charge is absorbed by M_8. Finally M_8 is opened by means of a slow gate transient to ensure low charge-injection on the input.

The chip has been processed by SGS-Thomson in $0.7\mu m$ CMOS digital process. The cell area is $65 \times 65\mu m^2$ giving a 390 dpi resolution level. A sample image produced for a 200×200 window is shown in Fig. 5 clearly showing grey levels. The image disappears as the finger is removed. The power consumption measured at $3\mu s$ of period cycle is $250\mu W$ for the digital circuitry and $300\mu W$ for the cell array and buffer. No light influence has been observed on the performance. Fig. 6 shows two superimposed output waveforms along with the charge sinking signal. The first output waveform displays two bumps related to the charge integration and to the charge sinking respectively. Conversely, the second waveform does not display the bump due to charge injection, demonstrating the effectiveness of the charge-injection compensation scheme. This issue is of great importance since the variation on the charge-injection signal contributes to the fixed pattern noise.

The die photograph of the sensor is displayed in Fig. 7.

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References:

1. C. Tsikos. Capacitive fingerprint sensor. *US patent 4,353,056.* October 5 1982.
2. A. G. Knapp. Fingerprint sensing device and recognition system having predetermined electrode activation. *US patent 5,325,442.* June 28 1994.

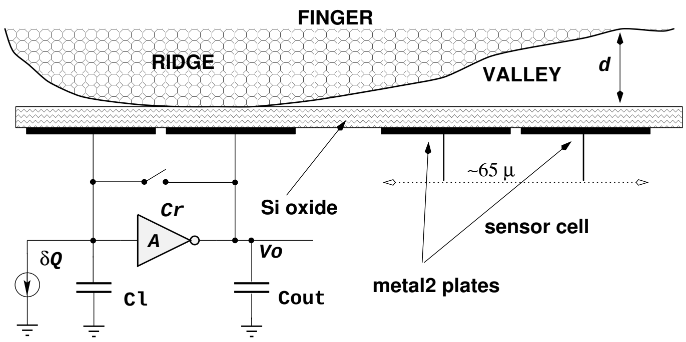

Figure 1: **Cross section and sensing principle of the cell.**

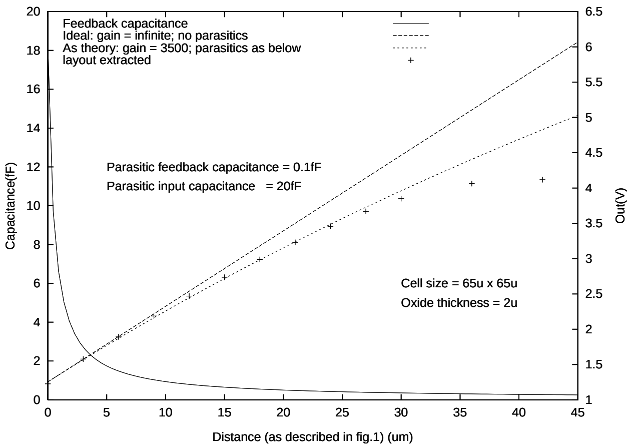

Figure 2: **Capacitive sensing simulations.**

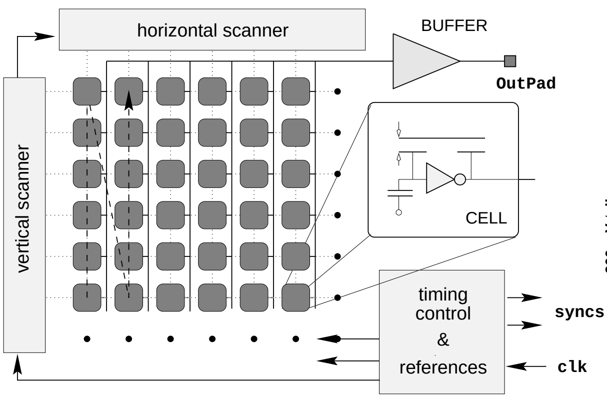

Figure 3: **Chip architecture.**

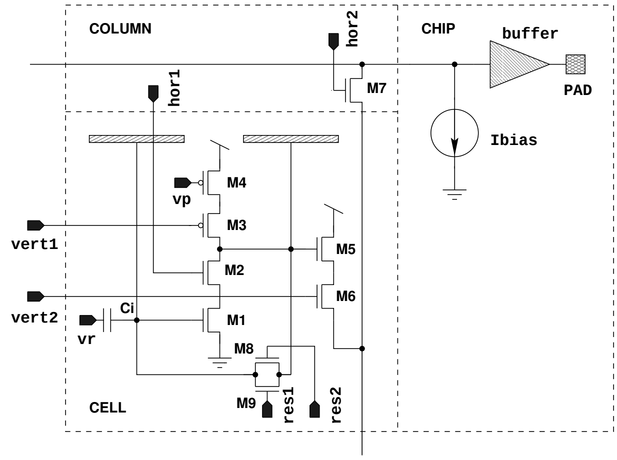

Figure 4: **Schematic of the cell and read-out circuitry.**

Figure 5: **Fingerprint image. This image has not been treated with any image processing.**

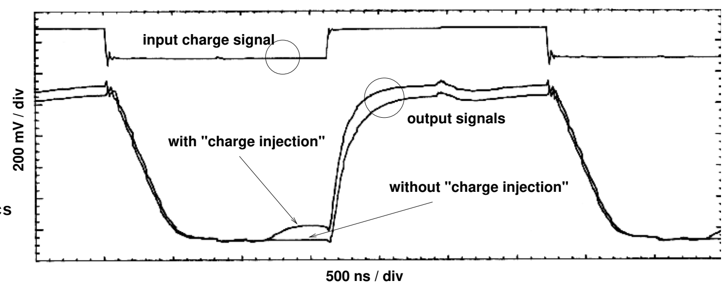

Figure 6: **Measurement of the output of the sensor.**