A Fingerprint Sensor Based on the Feedback Capacitive Sensing Scheme

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Abstract— **This paper introduces a single-chip, 200×200-element sensor array implemented in a standard 2-metal digital CMOS technology. The sensor is able to grab the fingerprint pattern without any use of optical and mechanical adaptors. Using this integrated sensor the fingerprint is captured at a rate of 10 F/s by pressing the finger skin onto the chip surface. The fingerprint pattern is sampled by capacitive sensors that detect the electric field variation induced by the skin surface. Several design issues regarding the capacitive sensing problem are reported and the feedback capacitive sensing scheme (FCS) is introduced. More specifically, the problem of the charge injection in MOS switches has been revisited for charge amplifier design.**

I. Introduction

BIOMETRIC systems are automated methods for verifying or recognizing the identity of a living person on the basis of some physiological characteristic. A range of biometric systems is now available with different tradeoffs involving component cost, reliability, discomfort in using the device, and other factors [1]. Among all, fingerprints have longest history of reliability.

Conventional forms of fingerprint sensing devices rely on optical detection methods. A simple optical sensing method can be open to fraudulent use by presenting a photographic image of a fingerprint. A more secure and common approach [2] is based on a glass prism with frustrated total internal reflection. Light is directed through one face, reflected at a second face and sensed at the third face. A finger is placed on the second face and at the points where the finger is in contact with the glass, i.e. at the ridges of the fingerprint, reflection no longer takes place. Light continues to be reflected where valleys of the fingerprint pattern are present. Light output from the third face is picked up by an image sensor. A binary image, where the fingertip in contact with the glass is shown as black and the rest as white, can therefore be obtained. Such an optical sensing device has disadvantages however. For example, the device is comparatively bulky. Also it is essential that the contact surface be maintained clean and free of dirt or grease. Moreover, some people have very dry fingers. Since a dry finger actually touches the glass at many fewer points than a moist finger, the lines of the fingerprint appear as rows of small dots so that more image processing becomes necessary.

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Integrated pressure sensors can overcome the above mentioned problems [3]. These sensors are based on a grid-like arrangement of polysilicon membranes electrically insulated from the underlying silicon substrate. When a finger exerts a force on the sensor, the lines and ridges on the tip of the finger touch the sensor elements, so that some membranes are deflected out of the quiescent position. By reading out the status of the membranes, an image of the line structure on the fingertip is obtained. The major problem of pressure sensors is that they require non-standard technology so that their cost is high.

This paper describes a sensor which uses a capacitive approach and avoids most of the aforementioned problems. Our fingerprint sensor is composed of an array of sensing elements connected to a read-out circuit. The cells are covered by dielectric material where a finger can be placed. Each element includes an active cell that detects the change of the electric field induced by the proximity of the fingerprint valleys to the cell plates. The presence of a finger overlying a sense electrode produces a capacitor whose capacitance is sensed. By measuring the different values of these capacitances, induced by the presence of ridges and valleys, an electronic representation of the fingerprint pattern can be obtained.

The idea of using a capacitive sensor array to detect fingerprints has been already described in [4], [5] but only one implementation [6], to our knowledge has been documented so far. In these designs the sensed capacitance is formed by a cell electrode and the respective overlying portion of the finger surface, presumably at ground potential (Fig.1A). The capacitance variation is sensed by a circuit external to the array. The main problem associated to this approach is related to the difficulty of sensing very small capacitances, typically varying between some tenths to a few fF. More specifically: 1) the signal, proportional to the value of the capacitance, is inversely proportional to the distance of the plates, i.e. the depth of the fingerprint valleys. This approach determines a strong non-linear output function versus the finger-sensor distance; 2) the small capacitance is sensed by applying a voltage step and by reading out the corresponding charge variation. This process is noisy and critical especially if performed by circuitry external to the cell array. In [6] this problem is tackled by increasing the voltage step, by decreasing the thickness of the insulating layer and by enlarging the size of the pitch. Unfortunately, this approach is in contrast with power optimization, reliability and image resolution.

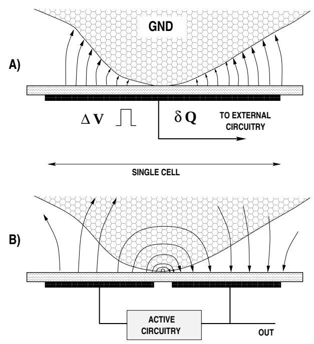

Fig. 1. Modes of implementation of surface capacitive sensors: state of the art (A) and proposed approach (B).

Our approach is based on two coplanar plates per cell that interact with the overlying portion of the finger surface (Fig.1B). The capacitance variation is sensed by a charge amplifier located in the cell area. Even if the capacitance per unit of area is reduced, by using this approach the small charge variation is sensed within the cell area, thus increasing the noise immunity and the robustness of the readout structure. Furthermore, there is no need of assuming the finger surface at ground potential as in the other approaches.

II. The FCS scheme

Fig.2 shows a generic charge amplifier scheme. The feedback capacitance C_r consists of three plates two of which are coplanar and facing the third one. If a δQ of charge is taken from the input, the following general expression of the output voltage can be derived:

$$\Delta V_o = \frac{\delta Q}{\frac{C_l}{A_0} + (1 + \frac{1}{A_0})C_r}; \tag{1}$$

where C_l is the input capacitance and C_r is the feedback capacitance. If the third plate is assumed floating, then C_r is composed of a parasitic capacitance C_p, due to the electric fringing field, and a term inversely proportional to the distance d, $(\epsilon_0 S)/(2d)$ where S is the plate area and d is the distance of the third plate from the first two. If the gain of the amplifier, $A_0 \gg 1$ and the fringing capacitance $C_p \ll C_r$ then eq. (1) becomes:

$$\Delta V_o \approx \frac{\delta Q}{C_r} = \frac{2\delta Q}{\epsilon_0 S} d;$$

showing a linear relationship of the output voltage versus distance d. A similar approach has been used, in a different context and by using alternate currents to measure distance between metal cutter blades [7].

The above technique has generated the cell architecture of Fig.3 where the third plate has been substituted by the skin surface. In order to fit a charge amplifier into the cell pitch, the differential amplifier shown in Fig.2 has been substituted by a high-gain inverter. The cell works in two phases: first, the charge amplifier is reset shorting the input and output of the inverter. During this phase, the output of the inverter settles to its logical threshold V_T. During the second phase, a fixed amount of charge δQ is sinked from the input causing an output voltage swing inversely proportional to the feedback capacitance value as explained above.

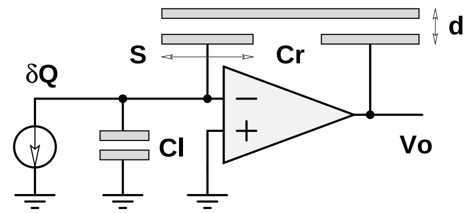

Fig. 2. Feedback capacitive sensing scheme.

In other words, for a fixed amount of sinked charge, the output voltage of the inverter will range between two extrema depending on the feedback capacitance value: i) the upper saturation level if no feedback capacitance is present; ii) a value close to the logical threshold when the feedback capacitance is large.

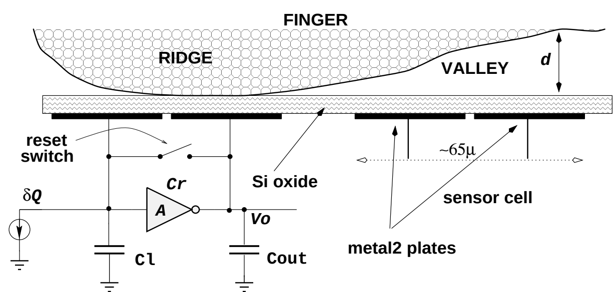

Fig. 3. Cross section of the capacitive sensing cell.

However, experiments have shown that the skin surface cannot be modeled as a floating gate and have proven that the feedback capacitance variation is due to different complex phenomena than what expected by the model of Fig.2. If no matter is present on the surface, the cell senses the parasitic capacitance induced by the fringing field as illustrated in Fig.4(A). Conversely, the cell senses the presence of an external body by means of a field shielding effect as in Fig.4(B) or by means of changes both of the field shape and of the dielectric constant as illustrated in Fig.4(C). Despite these complex relationships, measurements have proven the cell output monotonically related to the distance between the sensor surface and the skin.

III. Charge injection of the reset switch

Channel charge injection is one of the most important issues in the FCS scheme especially when small capacitance have to be sensed. The problem of charge injection of MOS switches has been extensively treated [8], [9], [10], but still lacks of detailed analysis regarding the feedback reset switch in charge amplifiers. More specifically, when the reset switch is active, there is a conduction channel that extends from the source to the drain of the transistor. When the gate voltage decreases, mobile carriers exit through

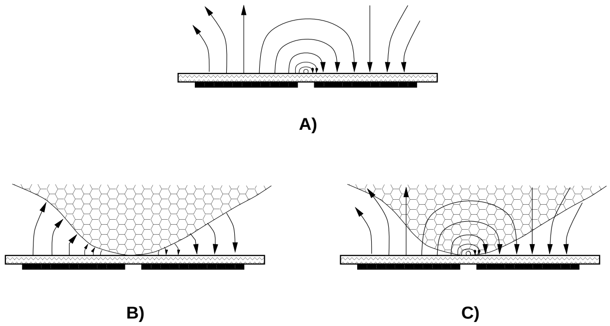

Fig. 4. Parasitic feedback capacitance (A) and sensing principle (B,C).

both the drain and the source end. The amount of channel charge that is injected into the input depends on several factors such as slope of the transient and input/output capacitance ratio. The problem can be generally neglected, but if the amount of channel charge is comparable to the charge amplifier sensitivity, as in our design, great care has to be taken to avoid spurious injection of charge into the input. The following analysis models the charge injection in charge amplifiers due to the reset-transistor, in order to define the correct policy of compensation. We will first analyze the channel charge behavior of a transistor switch shorting input and output of an amplifier, applying then the results to the charge amplifier case.

Fig.5 shows a single-pole model of an amplifier with gain $A_0 = g_m/g_o$ and gain-bandwidth product $GBW = g_m/C_o$ whose input and output are connected by an MOS transistor.

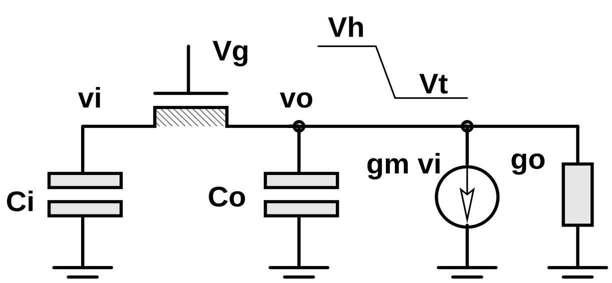

Fig. 5. Charge injection model of an MOS switch in the feedback loop of an amplifier.

Following the notation of the same figure, if we neglect charge pumping in the substrate and have large enough capacitor values $C_i, C_o \gg C_G$, where $C_G = WLC_{\mathrm{OX}}$ is the MOS gate capacitance, the potential profile can be assumed homogeneous along the channel [11]. If the above conditions are satisfied, the variation with time of the surface potential at any point of the channel is negligible with respect to that of the gate. Thus a linear decrease of V_G with slope U across the distributed gate capacitance C_G is equivalent to two symmetrical current sources of value $UC_G/2$ flowing to both ends [8]. Moreover, the above assumption will ensure a small value of $v_i - v_o$.

If we assume the transistor working in linear region and $|dV_G/dt| \gg |dv_i/dt|$, the Kirchkoff's current law (KCL) at the input node requires:

$$C_i \frac{dv_i}{dt} = -\beta(V_{HT} - Ut)(v_i - v_o) + \frac{C_G}{2}\frac{d(V_G - v_i)}{dt} =$$
$$\simeq -\beta(V_{HT} - Ut)(v_i - v_o) - \frac{C_G}{2}U. \qquad (2)$$

where v_i and v_o are the the input and output error voltages, $V_{HT} = V_H - V_S - V_T$ is the upper level of the transistor overdrive voltage, $\beta = \mu C_{\mathrm{OX}} W/L$, and $U = V_{HT}/t_d$ is the falling rate of the gate voltage during the switch off time t_d.

Similarly, KCL at the output node requires:

$$C_o \frac{dv_o}{dt} = \beta(V_{HT} - Ut)(v_i - v_o) - g_m v_i - g_o v_o - \frac{C_G}{2}U. \quad (3)$$

Equations (2) and (3) describe the dynamic behavior of the circuit of Fig.5. This equation can be numerically integrated between the time interval $[0, t_d]$ to determine the charge injected into the input. In order to derive a simpler mathematical description of the process we will approximate the above equations as follows.

If eq. (3) is added to eq. (2) we get:

$$C_G U + C_i \frac{dv_i}{dt} + C_o \frac{dv_o}{dt} + g_m v_i + g_o v_o = 0.$$

Integrating the above expression in the $[0, t]$ interval we obtain:

$$C_G U t + C_i v_i + C_o v_o + \int_0^t g_m v_i dt + \int_0^t g_o v_o dt = 0. \quad (4)$$

Equation (4) expresses the charge conservation principle of the circuit and can be used in place of eq. (3). Since v_i and v_o are monotonic functions of t, we assume a trapezoidal approximation for the integrals yielding:

$$C_G U t + C_i v_i + C_o v_o + \frac{g_m}{2} v_i t + \frac{g_o}{2} v_o t = 0. \qquad (5)$$

Substituting eq. (5) into eq. (2) and using the following non-dimensional variables:

$$\mathbf{T} = t\sqrt{\frac{\beta U}{C_i}}; \quad \mathbf{V} = v_i \sqrt{\frac{\beta C_i}{U}} / \frac{C_G}{2};$$

$$B = t_d \sqrt{\frac{\beta U}{C_i}} = \sqrt{\frac{\beta V_{HT} t_d}{C_i}}; \quad F = \frac{t_d}{1/GBW},$$

we get the normalized differential equation:

$$\frac{d\mathbf{V}}{d\mathbf{T}}\left(1 + \frac{F}{2A_0 B}\mathbf{T}\right) =$$
$$= (\mathbf{T} - B)\left[\left(1 + \frac{C_i}{C_o}\right)\mathbf{V} + 2\frac{C_i}{C_o}\mathbf{T} + \left(1 + \frac{1}{A_0}\right)\frac{F}{2B}\mathbf{T}\mathbf{V}\right] -$$
$$- \left(1 + \frac{F}{2A_0 B}\mathbf{T}\right). \qquad (6)$$

For $A_0 \gg F$, that is $t_d \ll C_o/g_o$, the equation simplifies to:

$$\frac{d\mathbf{V}}{d\mathbf{T}} = (\mathbf{T}-B)\left[\left(1+\frac{C_i}{C_o}\right)\mathbf{V} + 2\frac{C_i}{C_o}\mathbf{T} + \frac{F}{2B}\mathbf{T}\mathbf{V}\right] - 1. \quad (7)$$

In other words, if the gain of the amplifier is reasonably high at frequencies below the first pole, equation (7) can be taken as a good approximation of (6). As next step, if we further assume $g_m \to 0$, then $F \to 0$ and equation (7) simplifies to the normalized differential equation first introduced by Vittoz [9], [11] that describes a simple MOS switch with source and drain terminated on C_i and C_o (Fig.6):

$$\frac{d\mathbf{V}}{d\mathbf{T}} = (\mathbf{T}-B)\left[\left(1+\frac{C_i}{C_o}\right)\mathbf{V} + 2\frac{C_i}{C_o}\mathbf{T}\right] - 1 \qquad (8)$$

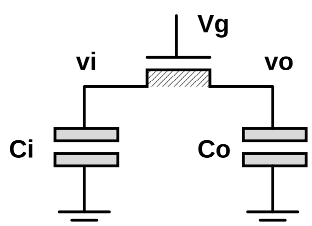

Fig. 6. Charge injection model of the switch: case $F = 0$, $A_0 = 0$.

Equations (6), (7) or (8), integrated between the initial time $\mathbf{T} = 0$ and the time at which the transistor is completely off $\mathbf{T} = B$, give the fraction of charge injected into the input node over the total channel charge, $(v_i C_i)/(V_{HT} C_G) = \mathbf{V}/(2B)$.

As already pointed out in [9] the B parameter, related to the square root of t_d, described by eq.(8), is the "driving force" of the switch-off process.

For the general case, the numerical integration of eq. (2) and (5) gives rise to the behavior plotted in Fig.7, where the plot derived by the integration of of eq.(8) is superimposed in dotted lines. As clearly illustrated, the transconductance g_m helps the channel charge to move to the output node. The actual charge partition is drastically modified from the case described by eq.(8): a part of the injected charge is removed by the transconductance and equipartition is not achieved for $C_i/C_o = 1$ in contrast with the model of the simple switch given by eq.(8). This effect becomes effective for large values of t_d.

The analysis of eq. (6) shows an additional "driving force" related to parameter F. To further emphasize this concept, the numerical integration of eq.(6) is plotted versus parameter F for fixed values of B in Fig.8. As clearly illustrated, even for high values of C_i/C_o increasing F greatly reduces the injection of charge into the input. This effect takes place for values of t_d that are one or two order of magnitude higher than $1/GBW$. The above plot also shows the weak role played by gain A_0 as predicted by the approximation introduced to derive eq. (7) from eq. (6). Hence eq.(7) can reasonably take place of eq. (7) for moderately high values of A_0.

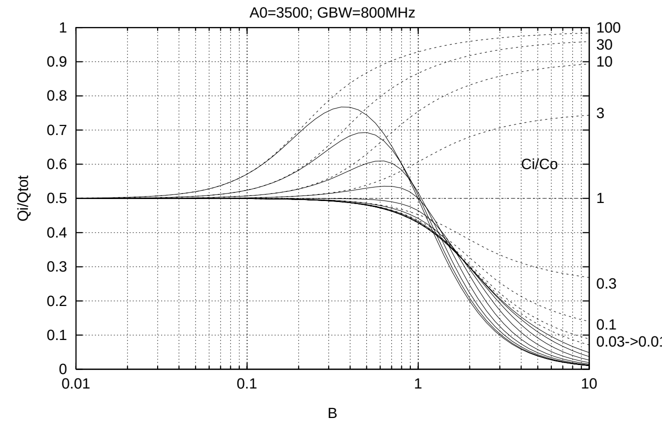

Fig. 7. Channel charge injected into the input node of the schematic of Fig.5 as result of the integration of eq. (2) and (5). $\beta = 63\mu A/V^2$, $C_G = 1.2fF$, $V_{HT} = 4.35V$, $g_m = 550\mu A/V$. Integration of eq.(8) is superimposed in dotted lines.

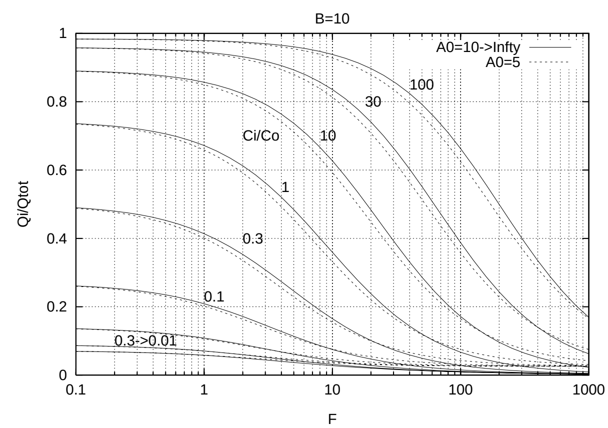

Fig. 8. Percentage of channel charge injected into the input of the circuit illustrated in Fig.5 versus the F parameter.

The analysis presented so far can be applied to the charge amplifier topology under certain conditions. Instead of introducing an additional term in equation (2), due to C_r, we will evaluate the conditions under which C_r can be introduced without affecting the previous analysis. Approximations will then be confirmed by SPICE simulations.

The settling time of the charge amplifier can be estimated as:

$$t_s = \frac{1}{\frac{g_o}{C_o}\left(1 + A_0\frac{C_r}{C_r+C_i}\right)} \simeq \frac{1}{GBW\frac{C_r}{C_r+C_i}}$$

Miller's theorem does not apply if the settling time of the charge amplifier is slower than the gate transition, that is $t_d \ll t_s$. This can be expressed by the following condition:

$$F = GBW t_d \ll \frac{C_r + C_i}{C_r}. \qquad (9)$$

If we add to the previous one the following:

$$C_r \ll C_i, C_o, \qquad (10)$$

we can assume that C_r plays a negligible role in charge sharing. This means that the switch-off process is composed of two phases. During the first one, since gate transition is faster than output settling, the charge is split between input and output in accordance to the previous analysis, thus determining a negligible voltage variation between v_i and v_o. During the second one, by virtue of the negative feedback, the input charge will be integrated onto C_r determining an output voltage step. This means that the above analysis is valid for slow gate transients, provided Millers' effect does not become effective.

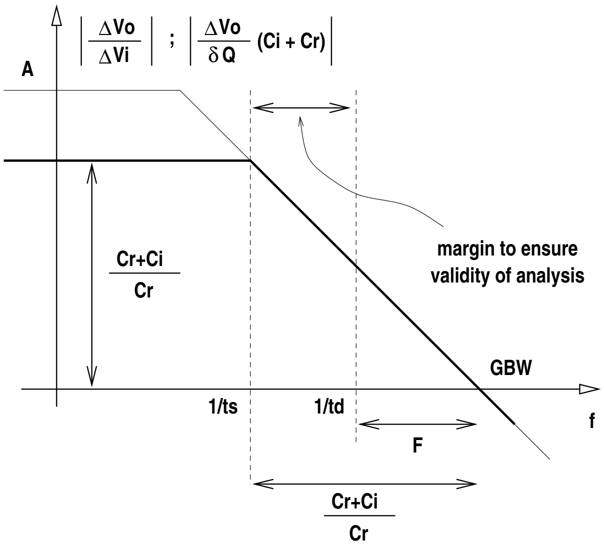

Fig. 9. Feedback in charge amplifiers. C_i and C_r are the input capacitance and feedback capacitance, respectively.

Condition (9) can also be displayed in a Bode plot as illustrated in Fig.9. The above figure shows how the gain plot of a single-pole amplifier changes when connected in a charge amplifier scheme. As the total gain is reduced to the inverse of the feedback loop gain, the pole moves toward the $GBWC_r/(C_r + C_i)$ point. The F parameter can be identified as the distance between the GBW point and the inverse of the switch-off time, t_d. Thus, condition (9) can be visualized as the distance between the two frequency points identified by the times t_s and t_d.

SPICE simulations have been performed to verify the above conditions and results are compared to the numerical solution of eq.(7) in Fig.10. The simulations parameters are appropriated for the sensor cell and conditions (9) and (10) have been verified for all the design cases. F is varied by changing t_d of an incremental factor. In order to keep parameters B, GBW, and A_0 constant, we have changed C_i, C_r, C_o, g_m, and g_o of the same factor in SPICE simulations. Overlap capacitances are set to zero since they are not taken into account in the analysis. The amount of charge injected into the input is calculated on both C_r and C_i. Due to the gain of the amplifier the plot of eq.(6) does not differ from the one of eq.(7).

To summarize, the following points have been shown: i) eq.(7) describes the behavior of the channel charge sharing when the amplifier input and output are connected. The above analysis can be extended to charge amplifiers if Miller's effect can be neglected by means of condition

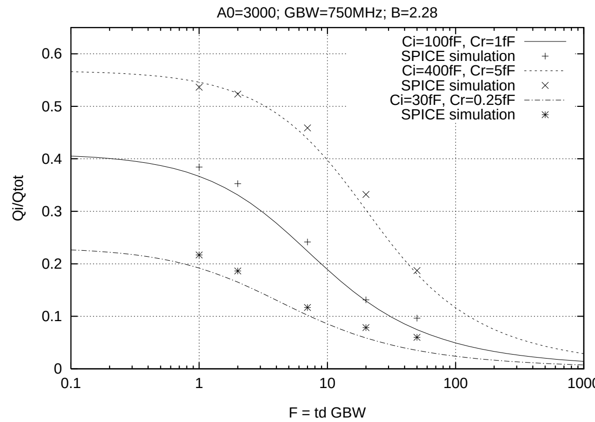

Fig. 10. Spice simulations compared to eq.(7) plots. For F=1: $g_m = 150\mu A/V$, $C_G = 8.45fF$, $V_{HT} = 4.35V$, $\beta = 95\mu A/V^2$ and $t_d = 1.3ns$, $C_o = 200fF$, C_i and C_r as in the plot keys.

(9). These conditions have been verified for several design cases by means of SPICE simulations. ii) The presence of conductance g_m in the model of the charge amplifier helps to drive the transistor channel charge away from the input node for large values of t_d; iii) this process is weakly related to the gain of the amplifier, but strongly related to its gain-bandwidth product.

IV. Charge injection compensation

Several strategies are available to reduce the amount of charge injected into the input of the charge amplifier by the reset transistor. Among them: i) size reduction of the reset transistor; ii) speed reduction of the switch off transient as analyzed in section III; iii) introduction of a complementary "dummy" transistor. Although used in literature [10], the latter approach has not been found suitable to our case. In fact, extensive circuit simulations have proven that the charge compensation is related to critical parameters, such as the transient time of the dummy transistor, to be reliable. This is particularly relevant when mismatch and process variations become significant.

To tackle the problem, we have chosen to maximize the gain-bandwidth product reducing the switch-off transient and size of the reset transistor, as previously derived. However, reducing the size of the reset transistor clashes with stability property of the amplifier during the reset phase, since reduces the loop gain bandwidth of the amplifier. For example, if we choose the cascode inverter topology, the frequency of the second pole is [12]:

$$\frac{1}{2\pi R_S C_{DG1}(1 + \frac{g_{m1}}{g_{m2}})};$$

where index 1 and 2 are related to the input and cascode transistors, respectively, and R_S is the input resistance given by the on-series resistance of the reset transistor. Therefore, reducing the size of the reset transistor, decreases phase margin of the system during the switch on.

The charge injection due to a minimum size reset transistor and due to a larger one that ensures suitable phase margin are plotted versus F by using eq.(7) in Fig.11. As clearly illustrated, the charge injection due to the wider one is not acceptable since the charge injected into the input for low values of F would saturate the output.

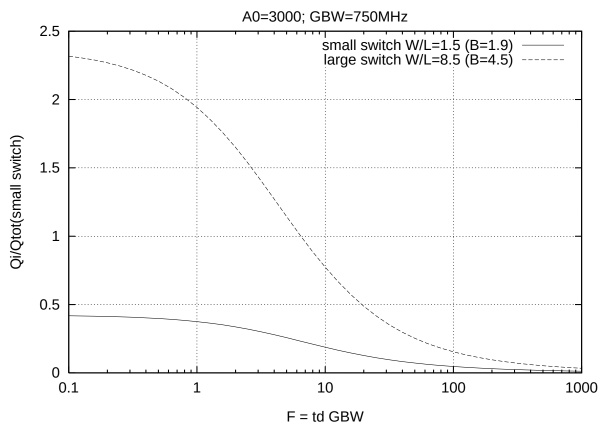

Fig. 11. Charge injection due to a minimum size reset transistor (solid line) and due to a wider transistor (dotted line), plotted versus the F parameter.

To overcome the trade-off between charge-injection and phase reduction, a *double reset scheme* as illustrated in Fig.12 has been used. It consists in introducing a second large switching transistor, activated at different phase than a smaller one. During the reset phase both transistors are set, reducing the resistance of the feedback loop, so that the output ringing is contained. During the charge integration phase, the large one is first opened so that its channel charge is absorbed by the other. Finally the small one is opened by means of a slow gate transient to ensure low charge-injection on the input.

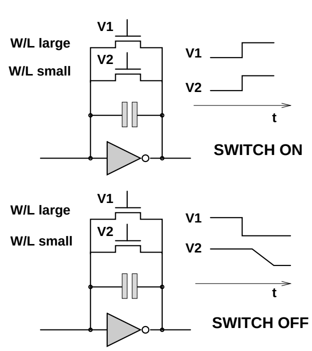

Fig. 12. The double reset scheme.

V. Implementation and measurement

A detailed schematic of the cell is illustrated in Fig. 13, where a cascode stage composed of M_1, M_2, M_3 and M_4 is used as high gain inverter. Two transistors of the cascode inverter M_2 and M_3 are used for addressing purposes, thus limiting power consumption. Shift registers address voltages between the supply rails by means of appropriate circuitry placed in the scanner array. When the cell is not addressed M_2 and M_3 turn off limiting the static current absorbed by the cell. The output of the inverter is buffered by a source follower stage M_5 into a vertical output line by means of M_6. Transistor M_7, which is addressed by the horizontal shift register, greatly reduces the output capacitance of the follower stage since only one vertical line is connected to the global output. The amount of charge required by the FCS scheme is simply injected into the input of the charge amplifier through a parasitic capacitance C_i when an internally generated voltage step is applied.

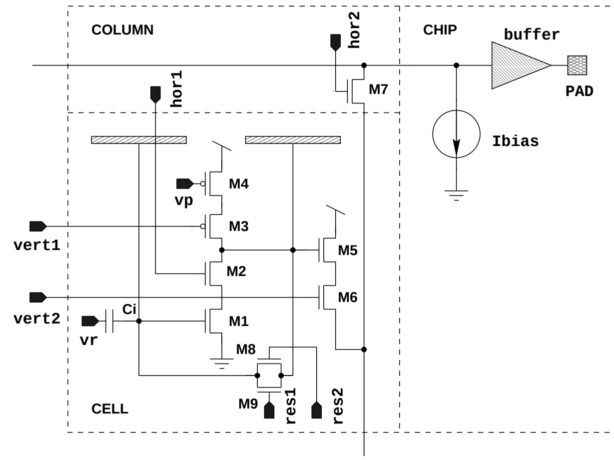

Fig. 13. Schematic of the cell.

Transistors M_8 and M_9 implement the *double reset scheme* as previously explained. The `res1` and `res2` signals are common to the whole array. In order to create a slow switch-off transient slope, a current source discharges the large capacitance composed of the sum of the M_8 gate capacitances over the whole array. A block diagram of the sensor is shown in Fig. 14. The array of cells is addressed in a raster mode by means of horizontal and vertical scanners. The chip also contains the timing control and voltage references to create waveforms needed for the *double reset scheme*. Signals activated every end-of-line and end-of-frame are automatically generated by the scanners and buffered to output pins to help image synchronization by external drivers.

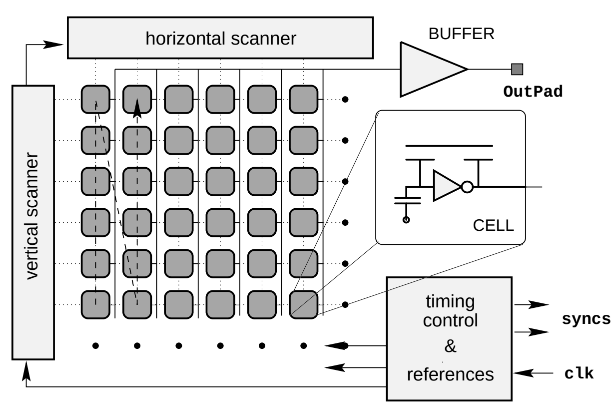

Fig. 14. Sensor architecture.

The chip has been processed by SGS-Thomson using a $0.7\mu m$ CMOS digital process. The cell area is $65 \times 65\mu m^2$

giving a 390 dpi resolution level. In Fig.15 a photograph of the chip, that measures $15 \times 15mm^2$, is shown.

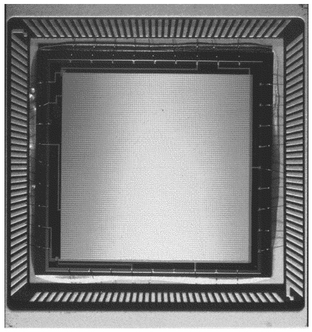

Fig. 15. Photograph of the chip.

Fig. 16 shows two superimposed output waveforms, related to the same pixel, along with the input charge signal. The first output waveform differs from the other in using a gate transient slope of the reset transistor two order of magnitude slower than the other. The *double reset scheme* used to compensate the charge injection problem has been found fully functional. The first output waveform displays two bumps related to the charge integration and to the charge sinking respectively while the second one does not. This issue is important since the variation of the charge injected contributes the fixed pattern noise. Experiments performed on the cell output have estimated the feedback capacitance in the $0.1 - 10fF$ range.

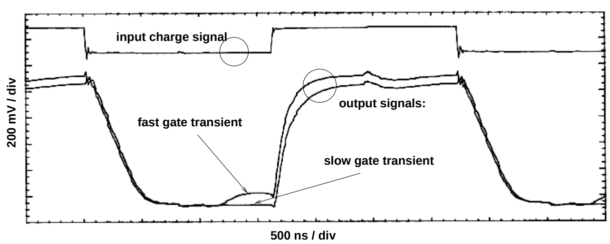

Fig. 16. Effectiveness of the double-reset scheme.

The overall performance of the sensor has been tested with a suitable A/D interface board so that images can be displayed and qualitatively compared in real time on a screen. To protect the bonding against the finger touch, we have deposited a thin epoxy glue layer around the array. No light influence has been observed on the performance when the sensor is not covered.

To test the behavior of the output of the cell versus distance of external matter, a conductive metal surface placed at different distances from the cell has been used. Following the analysis introduced in section II, an increasing number of fringing field lines are expected to be shielded by the metal surface as long as it approaches the sensor surface. In order to tackle the problem of setting very small distances, a calibrated sphere has been placed onto the top of the sensor so that a variable distance between the sensor and the metal surface can be sampled by the array. Since the distance gradually varies from the contact point according to a 2-D known relationship, the array will provide enough resolution to reconstruct the output versus distance behavior, if the radius of the ball is large. Several images taken from this experiment have been statistically treated and results displayed in Fig.17. The upper plot illustrates the relative output of the sensor versus distance for a wide range of distances while the bottom one is restricted to the smallest values. As clearly displayed, after a relatively linear behavior in the $[0 - 12]\mu m$ range the curve enters a saturated regime.

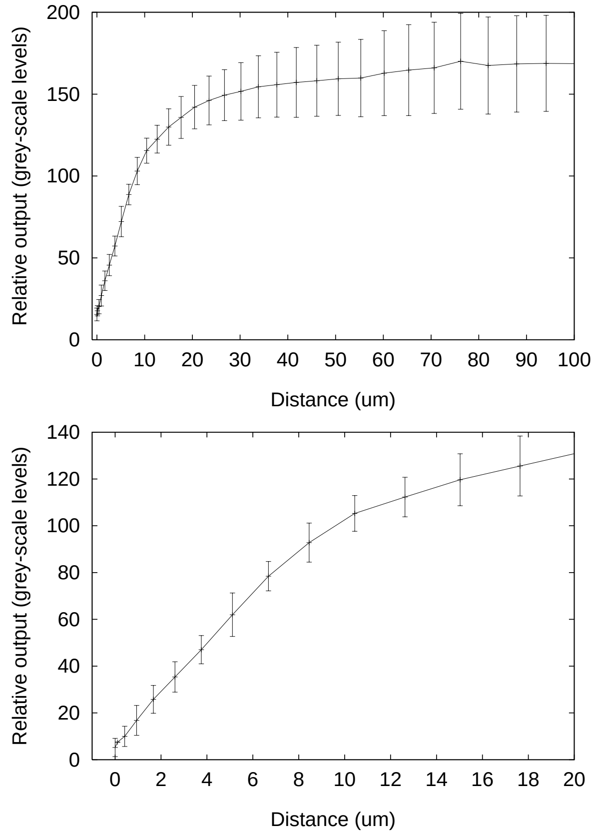

Fig. 17. Cell response versus distance of a conductive plane.

As introduced in section II, experiments have proven that human skin does not behave locally as a floating gate, as originally supposed, but behaves as illustrated in figures 4(B) and 4(C) according to the moisture level. A fingerprint image produced by a 200×200 window is shown in Fig. 18 along with enlarged subregions of the same image. In the left-side of the same figure the gray level function of the upper-left zoom is plotted in a 3D form to display the capability of the sensor to sense intermediate distance levels. The upper-right zoom shows how the pores of the skin are easily detected by the sensor resolution. Finally, whereas the glue is misplaced over the array, a uniform gray level is obtained, as displayed in the lower-right zoom.

The power consumption measured at $150\mu s$ of period cycle is $350\mu W$ for the digital circuitry and $900\mu W$ for the cell array and buffer. The characteristics of the sensor are summarized in Table I.

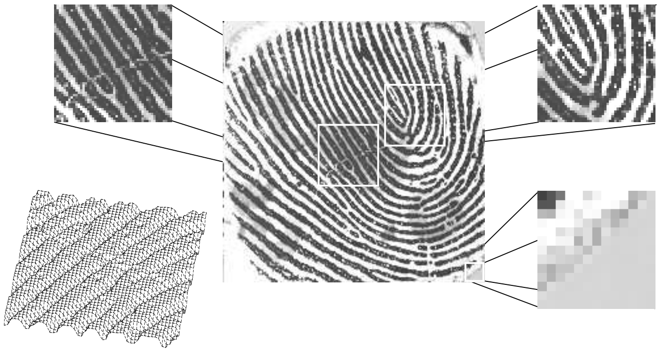

Fig. 18. Fingerprint raw image. It has not been treated with any image processing.

technology	2-metal $0.7\mu m$ digital cmos
die size	$15 \times 15mm^2$
array size	200×200
pixel pitch	$65\mu m$
frame rate	~ 10 F/s
energy consumption	$\sim 250\mu J$/acquisition

TABLE I

Characteristics of the sensor.

VI. Conclusion remarks

This paper has presented the design guidelines and test results of a capacitive fingerprint sensor. We introduced a differential capacitive sensing cell which is able to detect very small electric field variations induced by the fingerprint pattern. Since the channel charge injection of the reset switch in charge amplifiers is of capital importance for the correct behavior of the proposed cell, we analytically derived some constraints to compensate the above effect supporting the results with circuit simulations. Gray-level images have been shown, demonstrating a high level of detail.

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