Resume of Cecilia Metra

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Date and place of birth: Novembre 28th, 1965 in Borgo Val di Taro (Parma), Italy

Education:

- October 1995 – ***Ph.D.*** in Electronic Engineering and Computer Science, University of Bologna (Italy).
- December 1990 - ***Laurea in Electronic Engineering (summa cum laude)*** , University of Bologna (Italy).

Record of Emplyoment:

- 2005 – ***Associate Professor in Electronics*** at the Department of Electronics, Informatics and Systems (DEIS) of the University of Bologna.
- 2003 - Qualification as an ***Associate Professor in Electronics***.
- August – December, 2002 **- Visiting Faculty Consultant** for ***Intel Corporation (Santa Clara, CA).***
- June 2000 - Qualification as an ***Assistant Professor in Electronics.***
- September 1998 – September 2001 - **Visiting Professor** for the Department of Electrical Engineering of the ***University of Washington (Seattle, USA).***

Specializations and Research Interests:

- Design and Test of Digital Systems; Reliable and Error Resilient Systems; Fault Tolerance; On-Line Testing; Fault Modelling; Concurrent Diagnosis.

Editorials

- **Member of the Editor-In-Chief Search Committee** for the *"IEEE Transactions on Computers"*, February-March 2006.
- **Member of the Editorial Board** of the *"IEEE Transactions on Computers"*, starting from August 2004.
- **Member of the Editorial Board** of the *"Journal of Electronic Testing: Theory and Applications (JETTA)"*, starting from November 2004.

- **Member of the Editorial Board** of the International Journal *"Microelectronics Journal", Elsevier Science*, starting from January 2000.

- **Guest Co-Editor** of the**:**

  - **Special Issue** *on "Design and Test of Systems-On-a-Chip (SOC)"* of the **"IEEE Transactions on Computers",** May 2006 (together with JC Lo (University of Rhode Island, Rhode Island (USA) and F. Lombardi, Northeastern University, Boston (USA));.

  - **Special Issue** on *"On-Line Testing and Fault Tolerance"* of **"The Journal of Electronic Testing: Theory and Applications (JETTA)"**, 2005 (together with R. Leveugle, Imag, Grenoble (France));

  - **Special Issue** *on "Testing at MultiGbit/s Rates"* of the "**IEEE Design & Test"**, July-August, 2004 (together with A. Ivanov (British Coloumbia University, Vancouver (CA)) and F. Lombardi, Northeastern University, Boston (USA));

  - **Special Issue** on *"On-Line Testing"* of **"The Journal of Electronic Testing: Theory and Applications (JETTA)"**, 2004 (together with M. Sonza Reorda, Politecnico di Torino, Italy);

  - **Special Issue** on *the "8th IEEE International On-Line Testing Workshop"* of **"The Journal of Electronic Testing: Theory and Applications (JETTA)",** 2003 (together with M. Sonza Reorda, Politecnico di Torino, Italy);

  - **Special Issue** on *"Defect-Oriented Diagnosis for Very Deep Submicron Systems"* of the "**IEEE Design & Test"**, January-February, 2001 (together with F. Lombardi, Northeastern University, Boston, USA);

  - **Special Issue** on the *"7th IEEE International On-Line Testing Workshop"* of **"The Journal of Electronic Testing: Theory and Applications (JETTA)"**, Vol. 18, n. 3, June 2002 (together with D. Nikolos (Univ. of Patras, Greece), J. P. Hayes (Univ. of Michigan, USA) and M. Nicolaidis (iRoC Techn., France));

  - **Special Section** on "*Computer-Aided Design for Emerging Technologies*" of the "IEEE Design & Test", July-August 2007 (together with F. Lombardi, Northeastern Univ, Boston (USA)).

- **Invitation to nominee candidates for:**

  - *IEEE Computer Society Certificates of Appreciation* (1999)

  - *IEEE Transactions on VLSI Systems Best Paper Award* (1996)

- **Invited Paper** entitled: *"Majority Logic"* for the ***Wiley Encyclopedia of Electrical and Electronics Engineering, Wiley & Sons.,*** New York, Vol. 12, pp. 317--322, February 1999.

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Research Contracts' Responsability

- **Recipient** of a *Research Grant* from ***Intel Corporation (Santa Clara, CA),*** 2006.

- **Recipient** of a *Research Grant* from ***Intel Corporation (Santa Clara, CA),*** 2005.

- **Recipient** of a *Research Grant* from ***Intel Corporation (Santa Clara, CA),*** 2004.

- **Recipient** of an *Equipment Grant* from ***Intel Corporation (Santa Clara, CA),*** 2004.

- **Responsible** for the Research Contract with ***STMicroelectronics*** entitled: *"Modelling, Analysis and Fault Tolerance of Interconnects Among Different Cores of Systems in Package"*, 1 gennaio 2006 – 31 dicembre 2007.

- **Responsible** for the Research Contract with ***Intel Corporation (Hillsboro, Oregon)*** entitled: *"Development of Optimal Error Correcting Codes for Caches"*, 1 gennaio – 30 settembre 2006.

- **Responsible** of a Bologna Sub-Unit for a PNR 2005 project fundend by the **Italian Government** entitled "Architetture e componenti hw/sw ad elevata integrazione, sicurezza e modularità per i veicoli di nuova generazione", in collaboration with Fiat, Ferrari, Magneti Marelli, STMicroelectronics, ecc.

- **Responsible** for the Research Contract with ***STMicroelectronics*** entitled: *"Design and Testing Paradigms for Reliable Multiprocessor Systems"*, 2004-2006.

- **Responsible** of the Bologna Unit for a Research Contract fundend by ***the Italian Space Agency*** (ASI) 2005-2006.

- **Responsible** of the Bologna Unit for a PRIN project fundend by the **Italian Government** 2004-2006.

- **Responsible** of the Bologna Unit for the European Project (n. IST-2001-38782) fundend by the **European Community** within the Fifth Framework Programme entitled: *"Fault Tolerance: Electrical Aspects"*, coordinated by ***Philips Research Labs.,*** Eindhoven (The Netherlands), 2003-2004.

- **Responsible** of the Bologna Unit for the Research Contract fundend by ***the Italian Space Agency*** (ASI) entitled: "Definizione e sviluppo di tecniche di identificazione e tolleranza di guasti per la progettazione di sistemi di calcolo basati su componenti logici programmabili", 2000-2002.

- **Responsible** for the Research Contract with ***STMicroelectronics*** entitled: *"Design and Communication Paradigms for Reliable Automata Systems"*, 2000-2003.

- **Responsible** for the Research Contract with ***Alstom Transport*** entitled: *"Controllore di protocollo TFM self-checking in Tecnologia Field Programmable Gate Array (FPGA)",* 2001-2002.

- **Responsible** for the Research Contract with ***Alstom Transport*** entitled*: "Sistema di Verifica Funzionale per Apparati di Controllo Elettronico di Stazioni Ferroviari"*, 2002-2003.

Patents:

- **Co-inventor of** *"A Digital, Parallel, Clock Synchronizer"* (provisional US Patent OTT Ref #2505-3193).

- **Co-inventor** (together with Kleihorst Richard, Nieuwland Andre, Van Dijk Victor, ***Philips Research, Eindhoven, The Netherlands***) of a patent dealing with *Data Communication Using Fault Tolerant Error Correcting Codes and Having Reduced Ground Bounce* (International Publication Number WO 2005/088465 A1, International Publication Date 22 September 2005).

Professional Services (Conferences and Symposia)/Awards:

- ***IEEE Computer Society Meritorious Service Award***, 2006.

- ***IEEE Computer Society Certificate of Appreciation***, 2004.

- ***IEEE Computer Society Certificate of Appreciation***, 2000.

- **General Co-Chair** of the *"12th IEEE International On-Line Testing Symposium",* July 10-12, Lake of Como (Italy), 2006.

- **General Co-Chair** of *"The 20th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems"*, Monterey (California, USA), October 3-5, 2005.

- **Program Co-Chair** of the *"11th IEEE International On-Line Testing Symposium",* July 6-8, Cote Azur (France), 2005.

- **Program Co-Chair** of the *"10th IEEE International On-Line Testing Symposium",* July 12-14, Madeira (Portugal), 2004.

- **Program Co-Chair** of the *"10th IEEE International On-Line Testing Symposium",* July 12-14, Madeira (Portugal), 2004.

- **Program Co-Chair** of the *"9th IEEE International On-Line Testing Symposium",* July 7-9, Kos (Greece), 2003.

- **Program Co-Chair** of the *"8th IEEE International On-Line Testing Workshop",* July 8-10, Isle of Bendor (France), 2002.

- **General Co-Chair** of the *"7th IEEE International On-Line Testing Workshop",* July 9-11, Giardini Naxos-Taormina (Italy), 2001.

- **General Co-Chair** of *"The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems",* November 1-3, 1999, Albuquerque (New Mexico).

- **Program Co-Chair** of *"The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems"*, November 2-4, 1998, Austin (Texas)

- **Vice-Program Chair** of the *"6th IEEE International On-Line Testing Workshop",* July 3-5, 2000, Maiorca (Spain)

- **Vice-Program Co-Chair** of the *"5th IEEE International On-Line Testing Workshop",* July 5-7, 1999, Rhodes (Greece)

- **Vice-Program Co-Chair** of the *“4th IEEE International On-Line Testing Workshop",* July 6-8, 1998, Capri (Italy)

- **Member of the Steering Committee** of the *“The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems"* since May, 2001

- **Member of the Steering Committee** of the *“ACM Computing Frontiers Conference"* since May, 2003

- **Topic Coordinator** for *"On-Line Test",* for *"Fault Models”* and for *“Design For Availability”* of the:

  - ***IEEE International Test Conference (ITC) 2006,*** Santa Clara (California), October 22-27, 2006

  - ***IEEE International Test Conference (ITC) 2005,*** Austin (Texas), 6-10 November, 2005

  - ***IEEE International Test Conference (ITC) 2004,*** **Charlotte** (NC), 26-28 October, 2004

- **Topic Coordinator** for *"On-Line Test"* and for *"Fault Models”* of the:

  - ***International Test Conference (ITC) 2003,*** Charlotte (NC), 30 September - 2 October, 2003

  - ***International Test Conference (ITC) 2002,*** Baltimore (MD), October 8-10, 2002

  - ***International Test Conference (ITC) 2001***, Baltimore (MD), 30 October - 1 November, 2001

  - ***International Test Conference (ITC) 2000***, Atlantic City (NJ), 3-5 October, 2000

- **Topic Chair** for "On-line Testing, Fault Tolerance and reliability" of the ***“Design, Automation and Test in Europe (DATE) Conference",*** Nice (France), April 16-20, 2007

- **Topic Chair** for "On-line Testing, Fault Tolerance and reliability" of the ***“Design, Automation and Test in Europe (DATE) Conference",*** Munich (Germany), March 6-10, 2006

- **Topic Chair** for "On-line Testing, Fault Tolerance and reliability" of the ***“Design, Automation and Test in Europe (DATE) Conference",*** Munich (Germany), March 7-11, 2005

- **Topic Chair** for "Field-Oriented Test and On-line Testing" of the ***“Design, Automation and Test in Europe (DATE) Conference"***, Paris (France), February 16-20, 2004

- **Topic Chair** for "On-line Testing and Fault Tolerance" of the ***“European Test Symposium (ETS)”,*** Freiburg (Germany), May 20-24, 2007

- **Topic Chair** for "On-line Testing and Fault Tolerance" of the ***“European Test Symposium (ETS)”,*** Southampton (England), May 21-25, 2006.

- **Publicity Co-Chair of the *IEEE VLSI Test Symposium,*** Palm Springs (CA), May 1-5, 2005

- **Special Sessions Co-Chair of the *IEEE VLSI Test Symposium,* Berkeley (CA),** May 6 – 10, 2007

- **Special Sessions Co-Chair** of the ***IEEE VLSI Test Symposium,*** Berkeley (CA), April 30 – May 4, 2006

- **Member del Technical Program Committee** of the following International Conferences:

  - *The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Rome (Italy), September 26-28, 2007

  - *IEEE VLSI Test Symposium*, Berkeley (California), May 6—10, 2007

  - *1st IEEE International Workshop on Design for Manufacturability & Yield (DFM&Y 2006),* Santa Clara (California), October 26 – 27, 2006

  - *43rd Design Automation Conference,* San Francisco (California), July 24 – 28, 2006

  - *IEEE VLSI Test Symposium*, Berkeley (California), April 30 – May 4, 2006

  - *The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Washington DC (USA), October 4-6, 2006

  - *4th IEEE International Workshop on Infrastructure IP (I-IP),* Berkeley, California, USA, May 4-5, 2006

  - *3rd IEEE International Workshop on Silicon Debug and Diagnosis (SDD06),* Santa Clara (California), October 27 – 28, 2006

  - *IEEE International Workshop on Memory Technology, Design, and Testing (MTDT),* Tapei (Taiwan), August 3 – 5, 2005

  - *2nd IEEE International Workshop on Silicon Debug and Diagnosis (SDD05),* Austin (Texas), November 10 – 11, 2005

  - *IEEE VLSI Test Symposium*, Palm Springs (California), May 1 – 4, 2005

  - *IEEE European Test Symposium*, Talin (Estonia), May 22 – 25, 2005

  - *The 19th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Cannes (France), 10 – 13 October, 2004

  - *IEEE International Workshop on Memory Technology, Design, and Testing (MTDT),* San Josè (CA), August 9 – 10, 2004

  - *IEEE European Test Symposium*, Ajaccio, Corsica (France), May 23 – 26, 2004

  - *3rd IEEE International Workshop on Infrastructure IP (I-IP),* Palm Springs, California, USA, May 4-5, 2005

- *2nd IEEE International Workshop on Infrastructure IP (I-IP),* Charlotte, North Carolina, USA, October 28-29, 2004
- *1st IEEE International Workshop on Silicon Debug and Diagnosis (SDD04),* Ajaccio, Corsica (France), May 26 – 27, 2004
- *IEEE VLSI Test Symposium*, Napa (California), April 26 – 29, 2004
- *ACM Computing Frontiers Conference*, Ischia (Italy), April 14-16, 2004
- *IEEE VLSI Test Symposium*, Napa (California), April 27 - May 1, 2003
- *IEEE European Test Workshop*, Maastricht (The Netherlands), May 25 - 28, 2003
- *Design, Automation and Test in Europe (DATE) Conference*, Munich (Germany), March 3-7, 2003
- *The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Boston (MA), November, 2003
- *1st IEEE International Workshop on Infrastructure IP (I-IP),* Charlotte, North Carolina, USA, October 2-3, 2003
- *The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Vancouver (British Columbia), November 6-8, 2002
- *Design, Automation and Test in Europe (DATE) Conference*, Paris (France), March 4-8, 2002
- *IEEE International Workshop on Yield Optimization & Test*, Baltimore (MD, USA), November 1-2, 2001
- *Design, Automation and Test in Europe (DATE) Conference*, Munich (Germany), March 13-16, 2001
- *The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, San Francisco (CA), October 24-26, 2001
- *IEEE International Workshop on Yield Optimization & Test*, Atlantic City (NJ), October5-6, 2000
- *The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Mt. Fuji (Japan), October 25-27, 2000
- *Design, Automation and Test in Europe (DATE) Conference,* Paris (France), March 27-30, 2000
- *3rd IEEE International On-Line Testing Workshop,* Crete (Greece), July 7-9, 1997

- *The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Paris (France), October 20-22, 1997

- *2nd IEEE International On-Line Testing Workshop*, Saint-Jean de-Luz, Biarritz (France), July 8-10, 1996

- *The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Boston, Massachussets (USA), November 6-8, 1996

- *The IEEE International Workshop on Defect and Fault Tolerance in VLSI Systems*, Lafayette (Louisiana), November 13-15, 1995

- **Co-organizer of the following panels:**

  - *"Reliability Issues for Very Deep Submicron ICs",* of the *8th IEEE International On-Line Testing Workshop,* July 8-10, 2002, Isle of Bendor (France). The panel has been co-organized also with the international journal IEEE Design & Test.

  - *"Fault-Tolerance: needs and perspectives",* of the *IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems,* November 2-4, 1998, Austin (Texas). The panel has been co-organized also with the international journal IEEE Design & Test.

  - *"Yield, Testing and Reliability Issues for Very Deep Submicron Chips",* of the *IEEE International On-Line Testing Workshop,* July 9-11, 2001, Giardini Naxos-Taormina (Italy). The panel has been co-organized also with the international journal IEEE Design & Test.

- **Organizer of the following Special Sessions:**

  - "*Fault Tolerance Techniques for Memory Reliability Improvement"* for the ***IEEE International Workshop on Memory Technology, Design, and Testing (MTDT),*** San Josè (CA), August 9 – 10, 2004;

  - "*Robust Design Techniques for Soft Errors"* for the ***IEEE International On-Line Testing Symposium,,*** Saint Raphael (France), July 6 – 8, 2005;

  - *"Memory Reliability Challenges"* for the ***IEEE International On-Line Testing Symposium,*** Lake of Como (Italy), July 10 – 12, 2006;

  - *"Test and Reliability Challenges for Innovative Systems"* for the ***IEEE International On-Line Testing Symposium,,*** Saint Raphael (France), July 6 – 8, 2006.

- **Session Chair-Moderator** for the following International Conferences:

  - *Design, Automation and Test in Europe (DATE) Conference,* Nice (France), April 16-20, 2007

  - *43rd Design Automation Conference,* San Francisco (California), July 24 – 28, 2006

  - *12th IEEE International On-Line Testing Symposium,* July 10-12, Lake of Como (Italy), 2006.

- *IEEE VLSI Test Symposium*, Berkeley (California), April 30 – May 4, 2006

- *9th IEEE Workshop on Design and Diagnostics of Electronic Circuits and Systems* (DDECS'06), Prague (Czech Republic), April 18 – 21, 2006.

- *IEEE VLSI Test Symposium*, Palm Springs (California), May 1 – 4, 2005

- *IEEE International Workshop on Memory Technology, Design, and Testing (MTDT),* San Josè (CA), August 9 – 10, 2004

- *Design, Automation and Test in Europe (DATE) Conference***,** Munich (Germany), March 6-11, 2005

- *The 19th IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Cannes (France), 10 – 13 October, 2004

- *2nd IEEE International Workshop on Infrastructure IP (I-IP),* Charlotte, North Carolina, USA, October 28-29, 2004

- *IEEE VLSI Test Symposium*, Napa (California), April 26 – 29, 2004

- *ACM Computing Frontiers Conference*, Ischia (Italy), April 14-16, 2004

- *The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Boston (MA), November, 2003

- *1st IEEE International Workshop on Infrastructure IP (I-IP),* Charlotte, North Carolina, USA, October 2-3, 2003

- *IEEE European Test Workshop*, Maastricht (The Netherlands), May 25 - 28, 2003

- *IEEE International Workshop on Memory Technology, Design and Testing,* Isle of Bendor (France), July 10-12, 2002

- *8th IEEE International Mixed Signal Testing Workshop*, Montreux (Switzerland), June 18-21, 2002

- *IEEE European Test Workshop*, Corfù (Greece), May 26-29, 2002

- *20th IEEE VLSI Test Symposium,* Monterey (California), April 28 - May 1, 2002

- *4th International Conference on Massively Parallel Computing Systems (MPCS),* Ischia (Italy), April 10-12, 2002

- *Design, Automation and Test in Europe (DATE) Conference,* Paris (France), March 13-16, 2001

- *18th IEEE VLSI Test Symposium, Montreal (Canada),* April 30 - May 4, 2000

- *IEEE International Workshop on Yield Optimization & Test,* Atlantic City (NJ), October 5-6, 2000

- *6th IEEE International On-Line Testing Workshop*, Maiorca (Spain), July 3-5, 2000

- *5th IEEE International On-Line Testing Workshop,* Rhodes (Greece), July 5-7, 1999 *16th IEEE VLSI Test Symposium,* Monterey (California), April 26-30, 1998 *3rd IEEE International On-Line Testing Workshop*, Crete (Greece), July 7-9, 1997

- *The IEEE International Symposium on Defect and Fault Tolerance in VLSI Systems*, Paris (France), October 20-22, 1997

- **Reviewer for the following *International Conferences:***

  - *"International Test Conference"* (1997, 1998, 1999)

  - *"IEEE VLSI Test Symposium"* (1993, 1996, 1997, 1998, 1999, 2001, 2002)

  - *"The Seventh Asian Test Symposium"* (1998)

  - *"Design of Circuits and Integrated Systems Conference (DCIS98)"* (1998)

  - *"Power Timing Modeling Optimization and Simulation (PATMOS)"* (1997)

  - *"The IEEE International Symposium on Fault-Tolerant Computing"* (1995, 1996)

  - *"The European Design and Test Conference"* (1994)

Professional Societies

- **Vice Co-Chair** of th***e IEEE Computer Society Test Technololgy Technical Council (TTTC) Communications Group***, since 2004.

- **Vice Co-Chair** of the ***IEEE Computer Society Test Technololgy Technical Council (TTTC)Technical Activity Committee*** on ***"Defect Tolerance"***, since 2006.

- ***IEEE Computer Society Test Technololgy Technical Council (TTTC) Educational Program*** **Publicity Co-Chair*,*** since 2004.

- Member of the ***IEEE Computer Society Test Technololgy Technical Council (TTTC)*** **committee** on ***"Testing of Nano Devices and Systems"*** 2003-present.

- Member of the **1999 Technical Meeting Review Committee** of the ***IEEE Computer Society Test Technololgy Technical Council (TTTC).***

- Member of the **IEEE Computer Society.**

Invited Talks/Tutorials/Lessons:

- Invited Talk entitled: ***“Testing Clock Faults: Those That We Might Have Missed”, Intel Corporation, Santa Clara (CA),*** December 8th, 2004.

- Invited Talk "Testing e Design For Testability di Circuiti Elettronici Digitali", ***University of Padova (Italy),*** November 30, 2006.

- Invited Talk entitled: ***“Potentials of Fault Tolerance Paradigms for Scaled ICs’ Faults”, Intel Corporation, Santa Clara (CA),*** August 6th, 2004.

- Invited Tutorial on ***“Testing and Fault Tolerance", STMicroelectronics (Switzerland),*** April 6, 2004.

- Invited Talk "Collaudo e Progettazione Orientata al Collaudo di Sistemi Elettronici Digitali", ***University of Padova (Italy),*** December 1, 2005.

- Invited Talk entitled "Can High Performance Be Achieved Without Reliability Risks ?" at ***Philips Research Labs., Eindhoven (The Netherlands),*** March 17, 2003.

- Invited Talk entitled ***“Will Soft Errors Become a Problem and How Could We Solve It ?", Intel Corporation (MA),*** November 6, 2003.

- Invited Talk entitled *"Faults on the Clock Distribution Network and Their Impact on Testing"* at ***Artisan Components, Sunny Valley (CA, USA),*** November 21, 2002

- Invited Talk entitled *"Hardware Solutions for the Concurrent Detection of Transient, Crosstalk and Delay Faults in VDSM ICs"* at ***Agere Systems, Murray Hill (NJ, USA),*** May 17, 2001.

- Invited Talk entitled *"On-Line Testing for Logic Soft Errors: A Better Way",* at the ***Intel Test Research Symposium, Intel, Santa Clara (CA),*** September 29, 2000.

- Invited Tutorial entitled *"Hardware Fault-Tolerance: New Perspectives for Very Deep Sub-Micron Circuits ?",* at ***ST Microelectronics, Agrate (Milan, Italy),*** July 10, 2000.

- Invited Talk entitled *"Soft Errors' On-Line Testing: A Low Cost Approach",* at ***LogicVision, San Josè (CA),*** September 28, 2000

- Invited Talk entitled *"Concurrent Testing Techniques for Clock's Faults",* at the ***Intel Research Symposium VLSI Test, Intel, Santa Clara (CA),*** April 24, 1998.

- Invited Talk entitled *"Self-Checking Detectors for Faults Escaping Conventional Off-Line and On-Line Testing",* at ***The Boeing Company, Seattle (USA),*** October 27, 1998.

- Invited Lesson entitled *"Checker Design",* at the ***"European School on High Reliability Integrated Systems", Euroform,*** Bologna, February 9, 1994.

- Invited Lessons on "Reliability and Diagnostics", at the ***Corso di Perfezionamento Post-Laurea* of the *CEFRIEL, Politecnico of Milan*,** June 4-5, 2002.

- Invited Lessons on "Reliability and Diagnostics", at the ***Corso di Perfezionamento Post-Laurea* of the *CEFRIEL, Politecnico of Milan*,** June 4-5, 2002.

- **Panelist** for the panel entitled: ***"How can defect-based test be made to work in a foundry world ?"***, of the *IEEE International On-Line Testing Symposium*, 7-9 July, 2003, Kos (Greece), organized by R. Aitken, *Artisan Components (USA).*

Referreeing:

- **Reviewer for the following *Book and International Journals:***
  - *"CMOS Electronics. How it works. How it fails",* by J. Segura and C. Hawkins, published by the *IEEE Computer Society* (2003)
  - *"The IEEE Transactions on Computers"* (1995, 1996, 1997, 1998, 1999, 2000, 2001, 2002, 2003, 2004, 2005)
  - *"The IEEE Transactions on VLSI Systems"* (2003, 2004, 2005)
  - *"The IEEE Transactions on Reliability"* (2000, 2002, 2004)
  - *"IEEE Transactions on Device and Materials Reliability"* (2005)
  - *"IEEE Transactions on Instrumentation and Measurement"* (2001, 2002, 2003)
  - *"IEEE Transactions on Nuclear Science"* (2000)
  - *"IEEE Transactions on Computer-Aided Design"* (1998, 2002, 2003)
  - *"VLSI Design"* (1999)
  - *"IEEE Design & Test"* (1998, 1999, 2002, 2004, 2005)
  - *"The Journal of Electronic Testing: Theory and Applications (JETTA)"* (1996,2001, 2002, 2003, 2004, 2005)
  - *"International Journal of Systems Architectures"* (2001)
  - *"International Journal of Microelectronic System Integration"* (1997)

Grants:

- Grant from the *National Research Council* (Italy) - 1997

- Post PhD Grant from the *University of Bologna* (Italy) - 1996

- Grant from the *National Research Council* (Italy) - 1995

- PhD Grant from the *University of Bologna* (Italy) - 1992

- Grant from the *National Research Council* (Italy) - November 1991

- Grant from *SGS-Thomson* (Milan, Italy) - May 1991

Courses Taught:

- (Graduate) course on ***"High Reliability Electronics Systems"*** for the Specialistic Laurea Degree in Electronic Engineering of the ***University of Bologna*** for the Academic Year 2006-2007

- (Undergraduate) course ***"Electronics"*** for the Laurea Degree in Electrical Engineering of the ***University of Bologna*** for the Academic Year 2006-2007

- (Graduate) course on ***"High Reliability Electronics Systems"*** for the Specialistic Laurea Degree in Electronic Engineering of the ***University of Bologna*** for the Academic Year 2005-2006

- (Undergraduate) course ***"Digital Electronics"*** for the Laurea Degree in Computer Science Engineering of the ***University of Bologna*** for the Academic Year 2005-2006

- (Graduate) course on ***"High Reliability Electronics Systems"*** for the Specialistic Laurea Degree in Electronic Engineering of the ***University of Bologna*** for the Academic Year 2004-2005

- (Undergraduate) course ***"Digital Electronics"*** for the Laurea Degree in Computer Science Engineering of the ***University of Bologna*** for the Academic Year 2004-2005

- (Graduate) course on ***"High Reliability Electronics Systems"*** for the Specialistic Laurea Degree in Electronic Engineering of the ***University of Bologna*** for the Academic Year 2003-2004

- (Graduate) course on ***"High Reliability Electronics Systems"*** for the Specialistic Laurea Degree in Electronic Engineering of the ***University of Bologna*** for the Academic Year 2002-2003

- (Undergraduate) course ***"Analog Electronics"*** for the Laurea Degree in Computer Science Engineering of the ***University of Bologna*** for the Academic Year 2003-2004

- (Graduate) course ***"Reliability and Diagnosis of Electronic Compoenents and Circuits - Module I and Module II"*** for the Degree in Electronic Engineering of the ***University of Bologna*** for the Academic Year 2002-2003

- (Graduate) course ***"High Reliability Electronics Systems"*** for the Specialistic Laurea Degree in Electronic Engineering of the ***University of Bologna*** for the Academic Year 2002-2003

- (Graduate) course ***"Reliability and Diagnosis of Electronic Compoenents and Circuits - Module I"*** for the Degree in Electronic Engineering of the ***University of Bologna*** for the Academic Year 2001-2002

- (Undergraduate) course ***"Applied Electronics"*** for the Degree in Engineering for the Environment and Resources of the ***University of Bologna*** for the Academic Year 2001-2002

- (Undergraduate) course ***"Applied Electronics"*** for the Degree in Engineering for the Environment and Resources of the ***University of Bologna*** for the Academic Year 2000-2001

- (Undergraduate) course ***"Applied Electronics"*** for the Degree in Engineering for the Environment and Resources of the ***University of Bologna*** for the Academic Year 1999-2000

- (Undergraduate) course ***"Applied Electronics"*** for the Degree in Engineering for the Environment and Resources of the ***University of Bologna*** for the Academic Year 1998-1999

- (Undergraduate) course ***"Automatic Design of Electronic Circuits and Systems"*** for the degree in Electronic Engineering of the ***University of Udine*** for the Academic Year 1995-1996

Graduate Students and Research Associate Supervision:

- **Ph.D. Degree Supervision:**

  - Eng. Daniele Rossi, DEIS - University of Bologna (Italy), in progress.

  - Eng. Martin Omaña, DEIS - University of Bologna (Italy), in progress.

  - Eng. Josè Manuel Cazeaux - DEIS - University of Bologna (Italy), in progress.

- **External reviewer for the Ph.D.** in Computer Science of the University of Verona (Italy) of A. Fin, entitled *"A Functional Testing Framework for Embedded Systems"*.

- **Research Associate Supervision:**

  - Eng. Andrea Pagano, DEIS - University of Bologna (Italy), 2001

  - Eng. Luca Schiano, DEIS - University of Bologna (Italy), 2001-2002

  - Eng. Stefano Di Francescantonio, 2001 – 2003

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