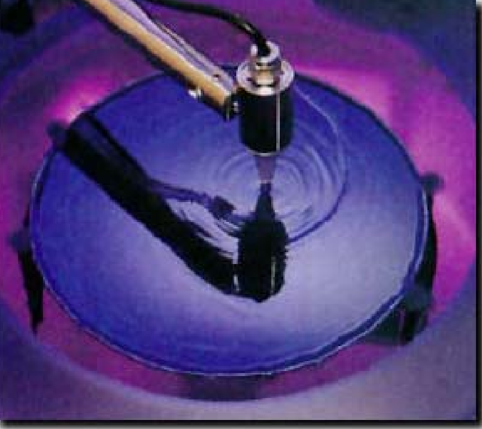


Introduction to VLSI Fabrication Technologies

Emanuele Baravelli

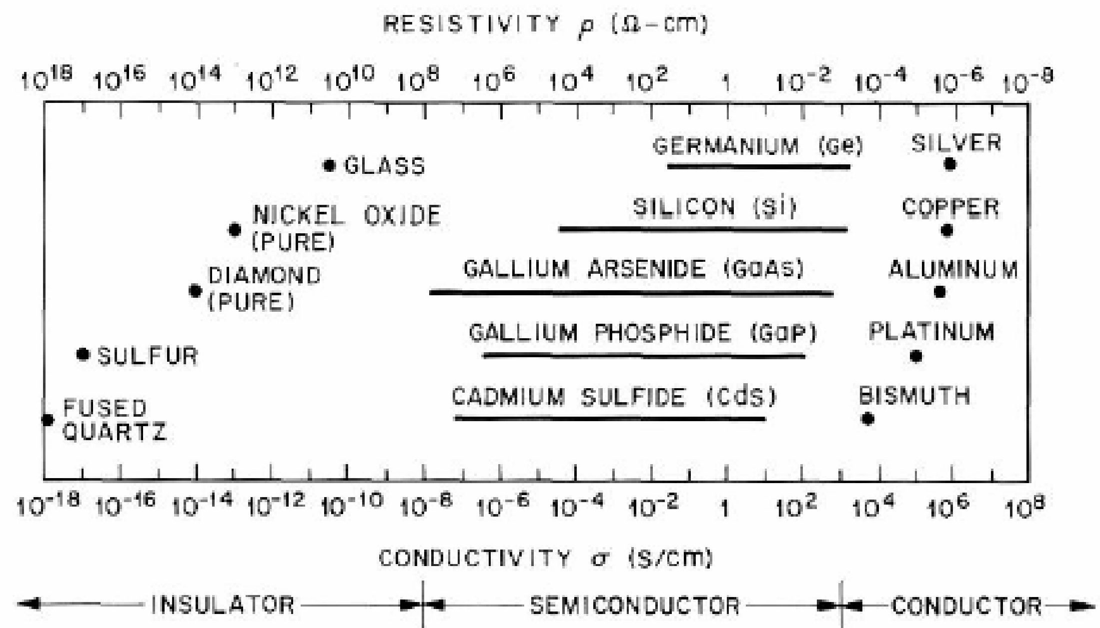
Organization

- Materials Used in VLSI Fabrication
- VLSI Fabrication Technologies
- Overview of Fabrication Methods
- CMOS Process Stages

Main Categories of Materials

Materials can be classified into three main groups regarding their electrical conduction properties:

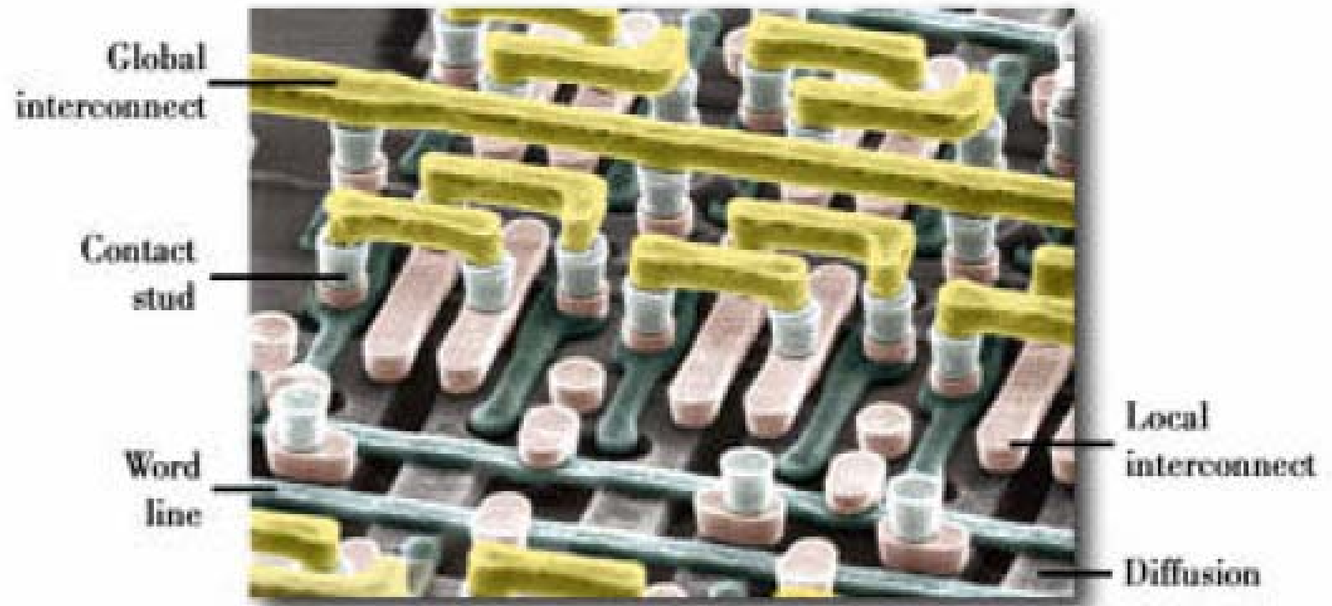
- **Insulators**
- **Conductors**
- **Semiconductors**



Conductors

Conductors are used in IC design for electrical connectivity. The following are good conducting elements:

- **Silver**
- **Gold**
- **Copper**
- **Aluminum**
- **Platinum**

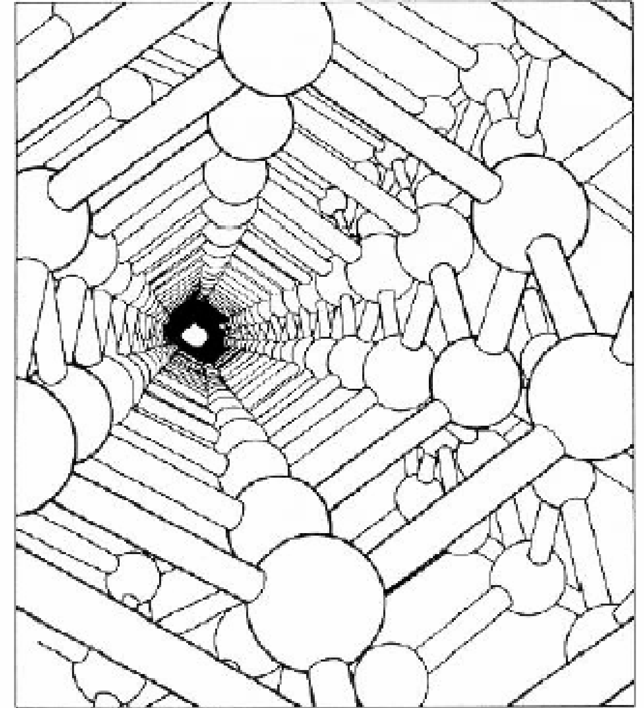


Insulators

- Insulators are used to isolate conducting and/or semi-conducting materials from each other.
- MOS devices and Capacitors rely on an insulator for their physical operation.
- The choice of the insulators (and the conductors) in IC design depends heavily on how the materials interact with each other, especially with the semiconductors.

Semiconductors

- The basic semiconductor material used in device fabrication is **Silicon**
- The success of this material is due to:
  - Phisical characteristics
  - Abundance in nature and very low cost
  - Relatively easy process
  - Reliable high volume fabrication



- Other semiconductors (e.g. GaAs) are used for special applications

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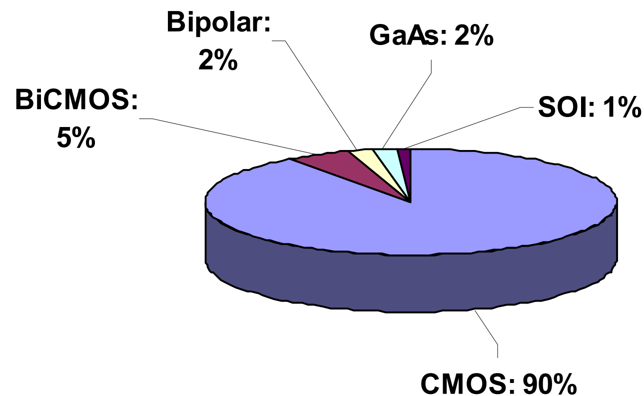
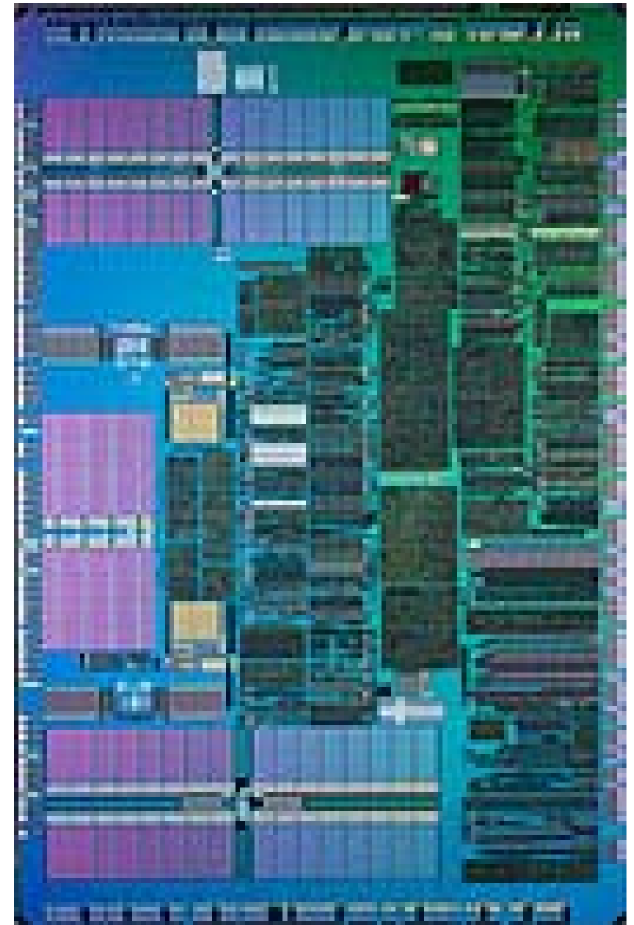
Overview of Processing Technologies

Although a number of processing technologies are available, the majority of the production is done with traditional CMOS. Other processes are limited to areas where CMOS is not very suitable (like high speed RF applications)

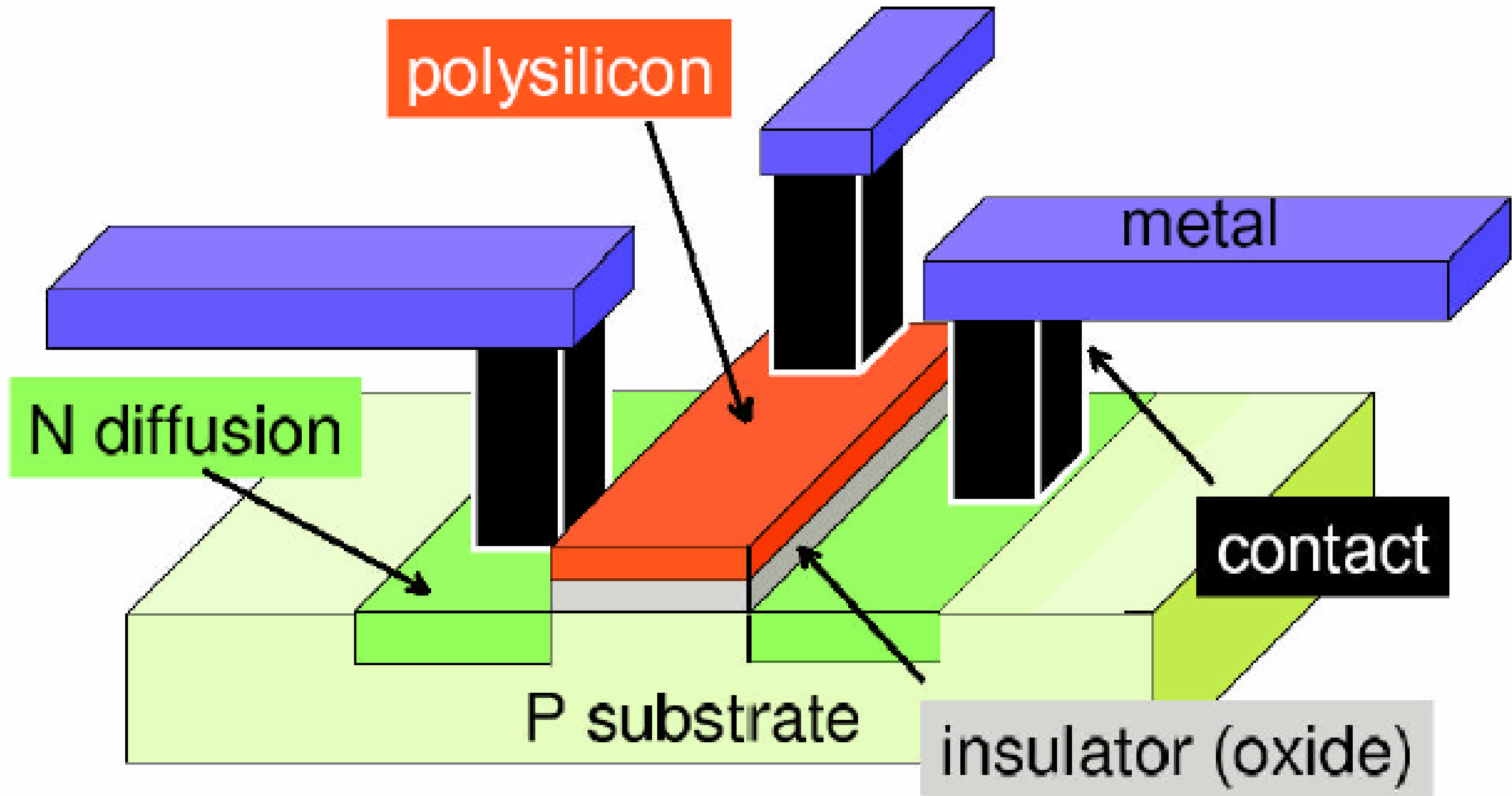


CMOS technology

- An **Integrated Circuit (IC)** is an electronic network fabricated in a single piece of a semiconductor material
- The semiconductor surface is subjected to various processing steps in which impurities and other materials are added with specific geometrical patterns
- The fabrication steps are sequenced to form three dimensional regions that act as transistors and interconnects that form the network

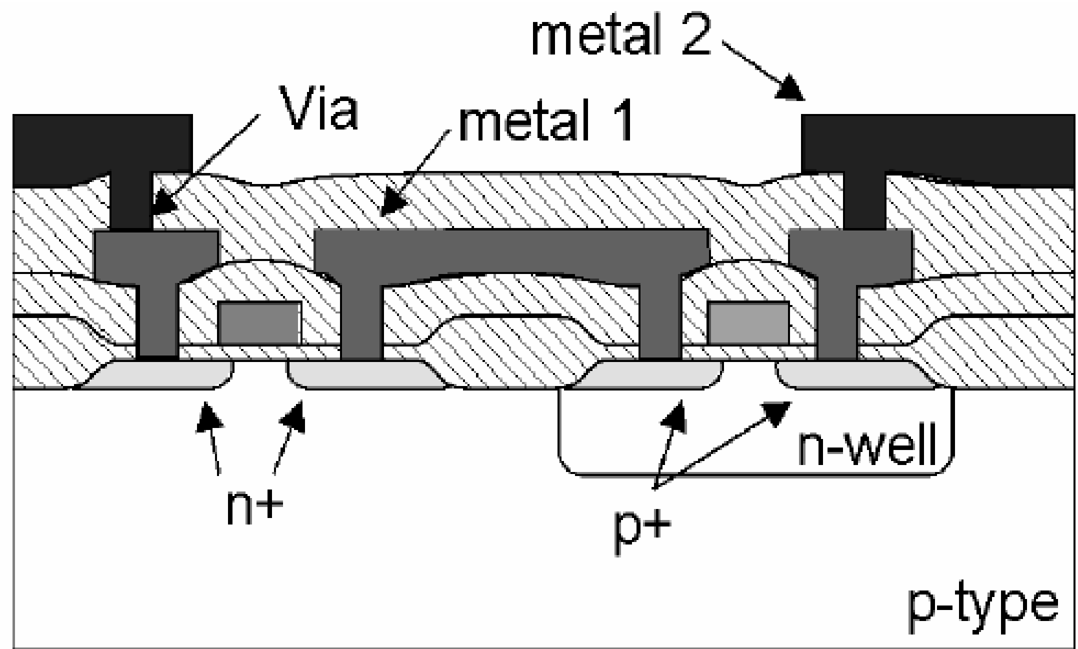


Simplified View of MOSFET



CMOS Process

The CMOS process allows fabrication of nMOS and pMOS transistors side-by-side on the same Silicon substrate.



Organization

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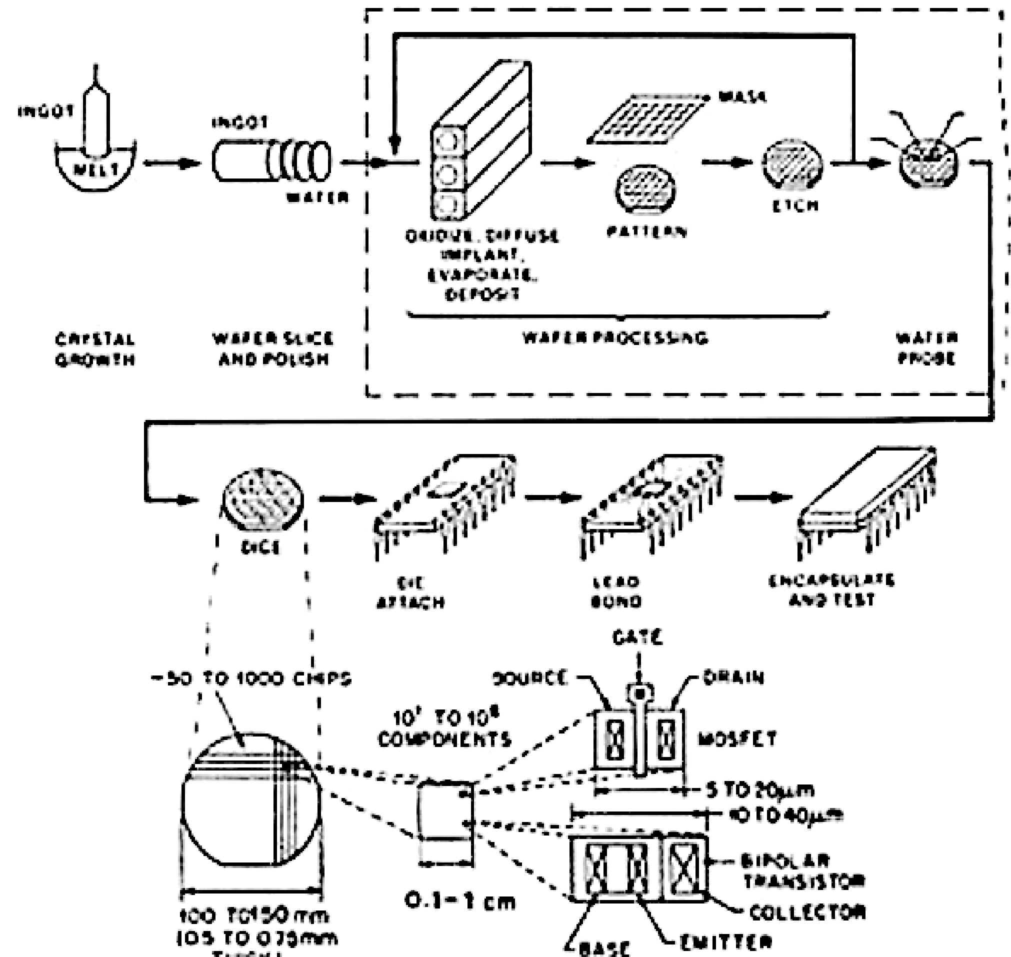
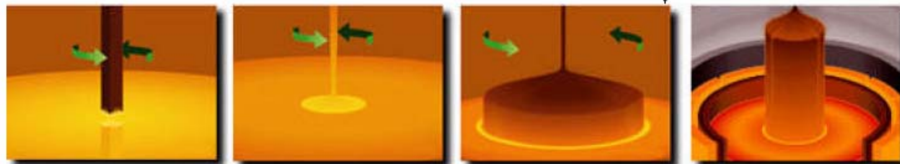
Fabrication process sequence

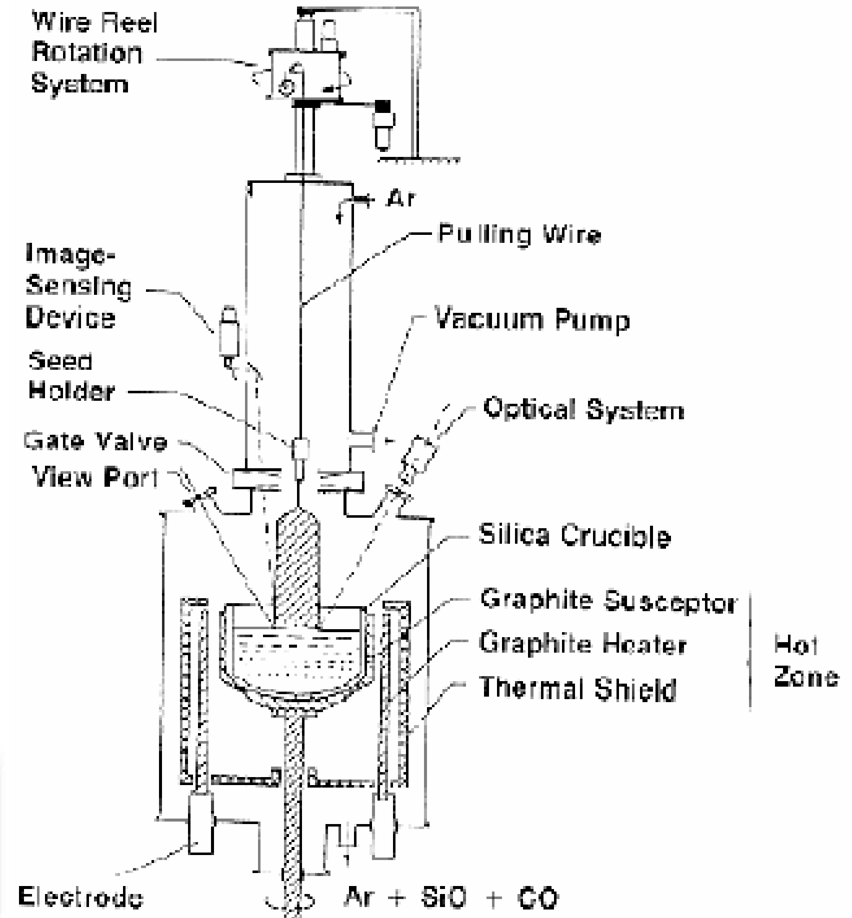
- Silicon manifacture
- Wafer processing
  - Lithography
  - Oxide growth and removal
  - Diffusion and ion implantation
  - Annealing
  - Silicon deposition
  - Metallization
- Testing
- Assembly and packaging



Single Crystal Growth (I)

- Pure silicon is melted in a pot (1400º C) and a small seed containing the desired crystal orientation is inserted into molten silicon and slowly (1mm/minute) pulled out

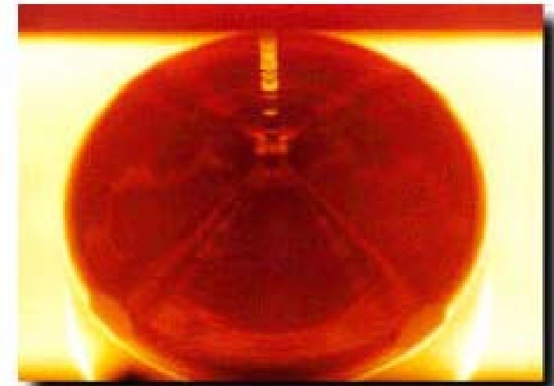




Single Crystal Growth (II)

- The silicon crystal (in some cases also containing doping) is manufactured as a cylinder (**ingot**) with a diameter of 8-12 inches (1”=2.54 cm).
- This cylinder is carefully sawed into thin (0.50-0.75 mm thick) disks called **wafers**, which are later polished and marked for crystal orientation.

Single Crystal Silicon Ingot



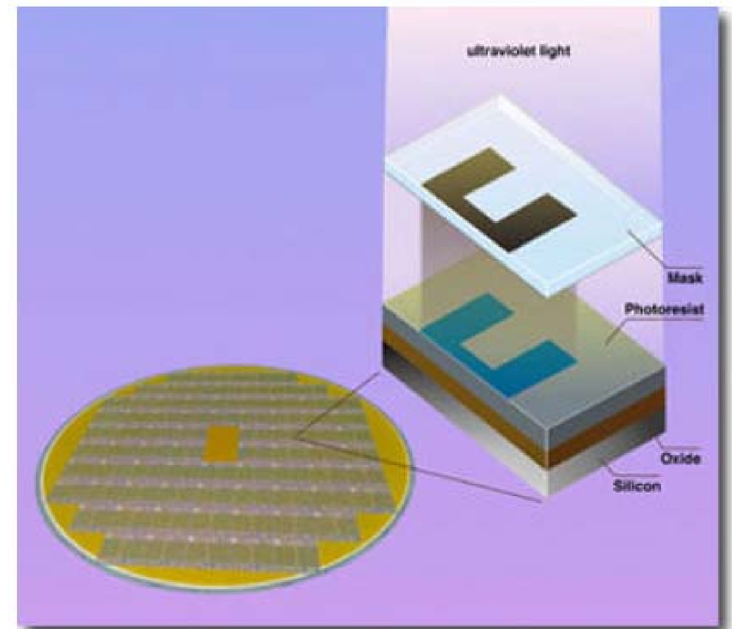
Inside CZ Puller
(MEMC)

Lithography (I)

Lithography: process used to transfer patterns to each layer of the IC

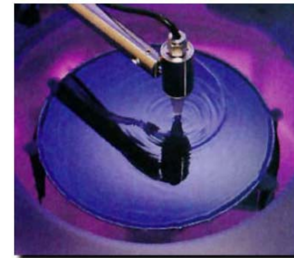
Lithography sequence steps:

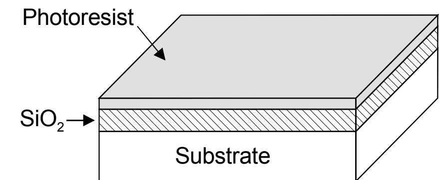
- Designer:
  - Drawing the "layer" patterns on a layout editor
- Silicon Foundry:
  - Masks generation from the layer patterns in the design data base
  - Printing: transfer the mask pattern to the wafer surface
  - Process the wafer to physically pattern each layer of the IC



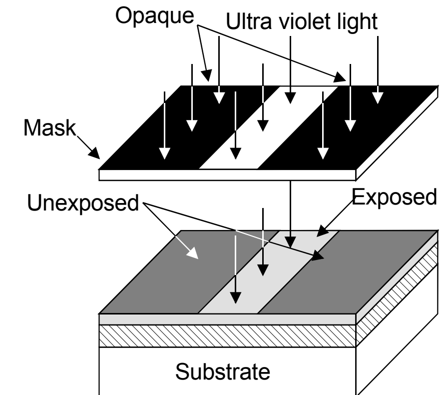
Lithography (II)

1. <u>Photoresist application:</u>
   - the surface to be patterned is spin-coated with a light-sensitive organic polymer called photoresist

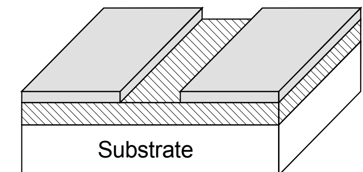




2. <u>Printing (exposure):</u>
   - the mask pattern is developed on the photoresist, with UV light exposure
   - depending on the type of photoresist (negative or positive), the exposed or unexposed parts become resistant to certain types of solvents



3. <u>Development:</u>
   - the soluble photoresist is chemically removed
   - The developed photoresist acts as a mask for patterning of underlying layers and then is removed.

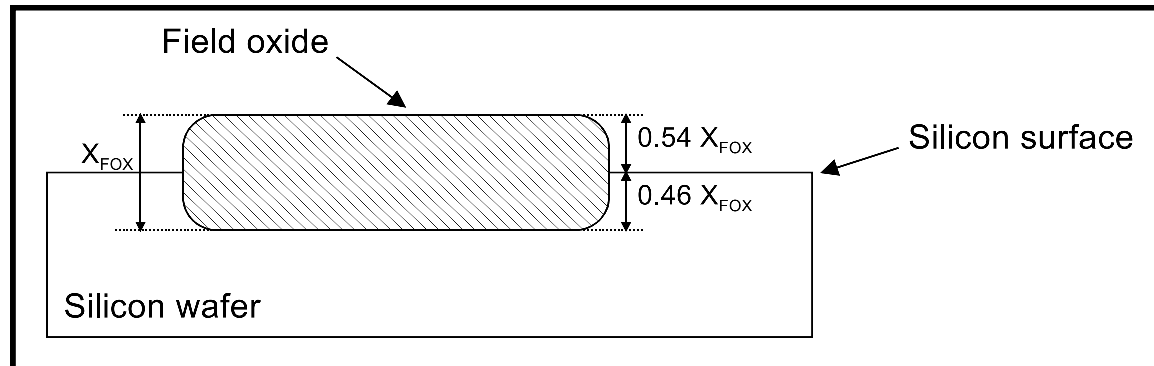


Oxide Growth / Oxide Deposition

- Oxide can be **grown** from silicon through heating in an oxidizing atmosphere
  - Gate oxide, device isolation
  - Oxidation consumes silicon

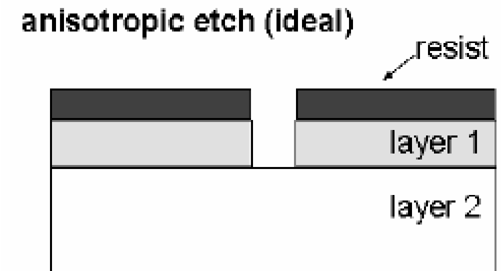
Oxidation Furnace
(Silicon Valley Group - Thermco Systems)

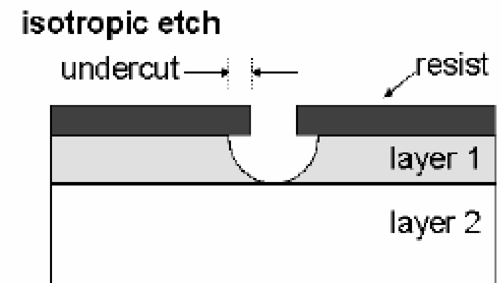
- SiO_2 is **deposited** on materials other than silicon through reaction between gaseous silicon compounds and oxidizers
  - Insulation between different layers of metallization

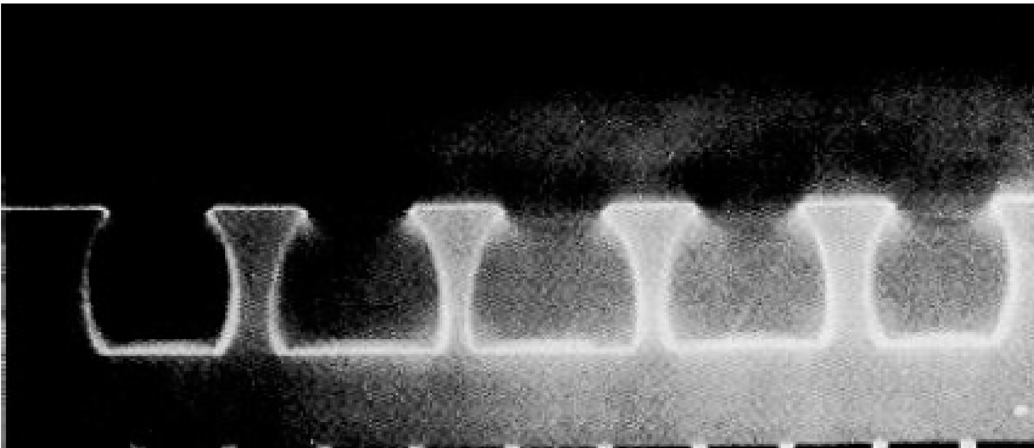


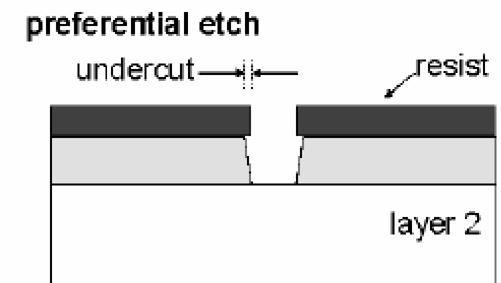
Etching

- Once the desired shape is patterned with photoresist, the **etching** process allows unprotected materials to be removed
  - Wet etching: uses chemicals
  - Dry or plasma etching: uses ionized gases



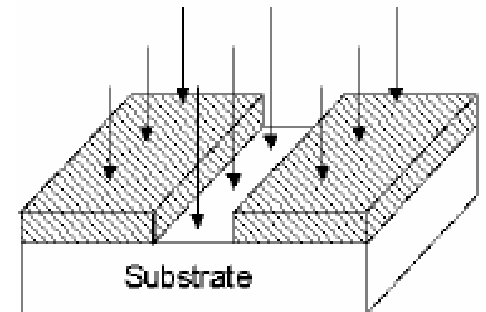




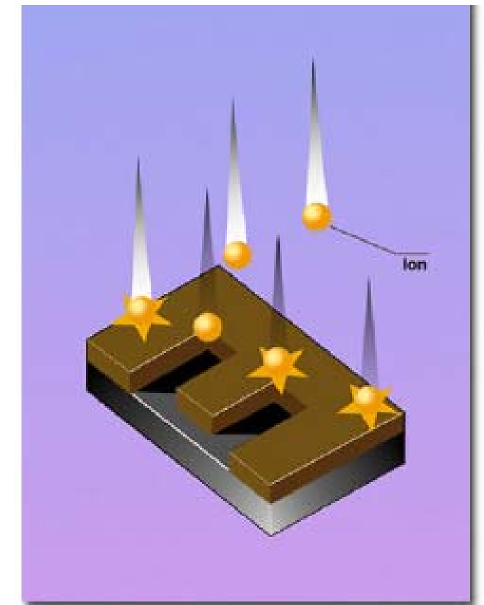


Diffusion and Ion Implantation

Doping materials are added to change the electrical characteristics of silicon locally through:



- **Diffusion**: dopants deposited on silicon move through the lattice by thermal diffusion (high temperature process)
  - Wells
- **Ion implantation**: highly energized donor or acceptor atoms impinge on the surface and travel below it
  - The patterned SiO_2 serves as an implantation mask
  - Source and Drain regions



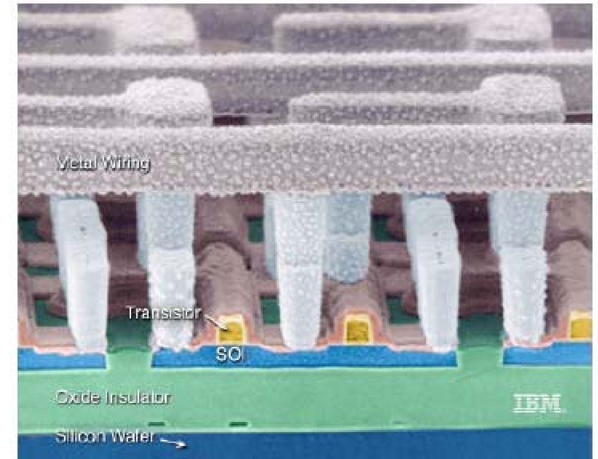
Annealing

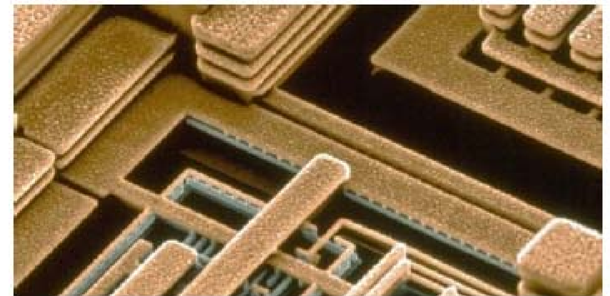
Thermal annealing is a high temperature process which:

- allows doping impurities to diffuse further into the bulk
- repairs lattice damage caused by the collisions with doping ions

Silicon Deposition and Metallization

- Films of silicon can be added on the surface of a wafer
  - **Epitaxy**: <u>growth</u> of a single-crystal semiconductor film on a crystalline substate
  - **Polysilicon**: polycrystalline film with a granular structure obtained through <u>deposition</u> of silicon on an amorphous material
    - MOSFET gates
- Metallization: deposition of metal layers by evaporation
  - interconnections





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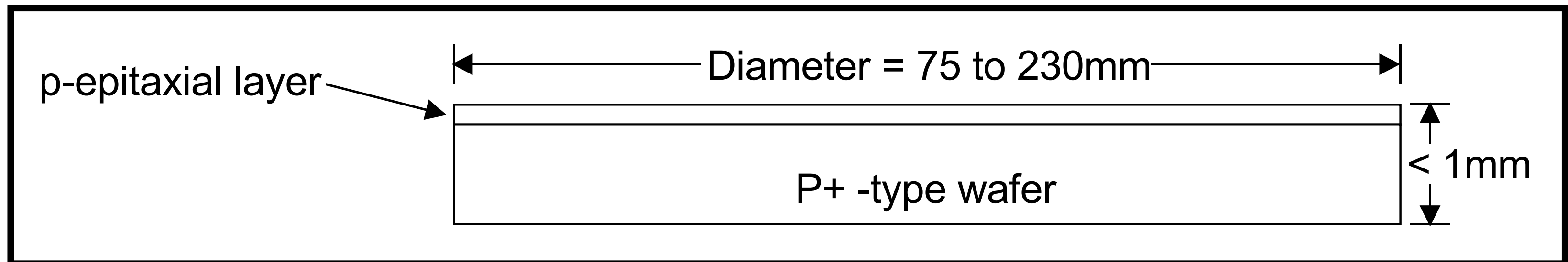
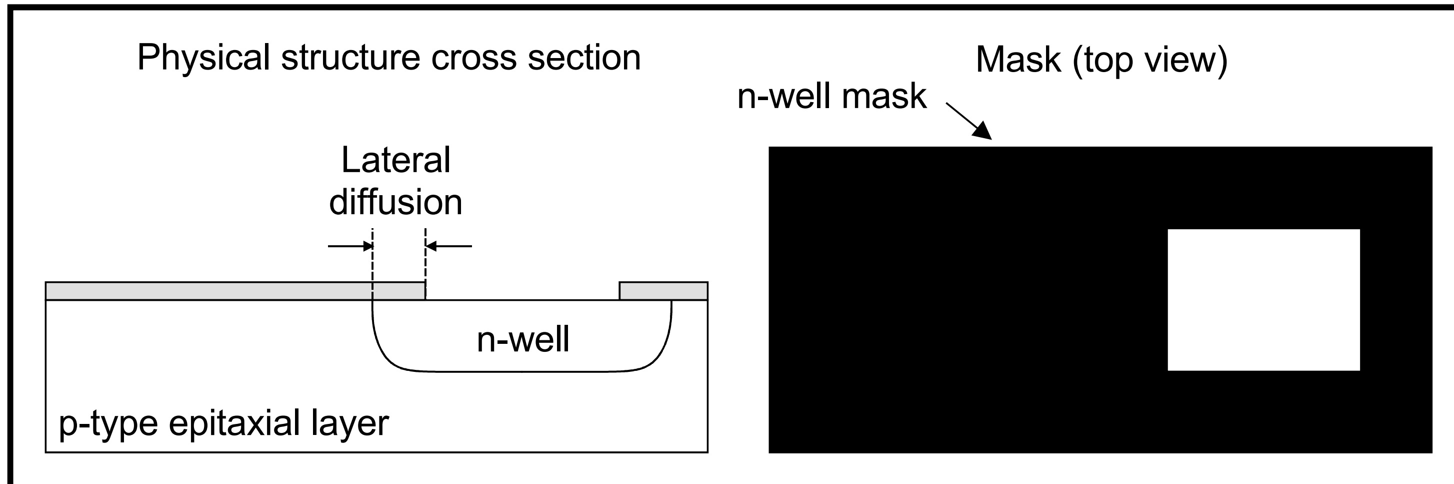
1. Epitaxial growth

- A p-silicon epitaxial layer is grown on the surface of a p-type wafer
- The epi layer is used as the base layer to build the devices



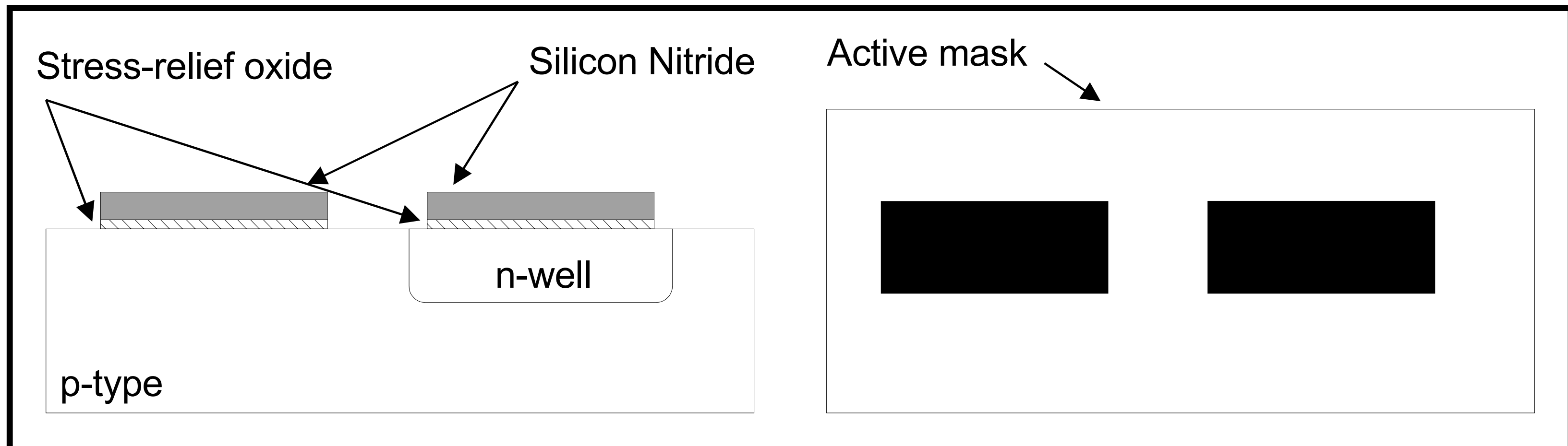
2. N-well Formation

- The first mask defines the n-well regions for pMOS transistors
- n-well's are formed by ion implantation or deposition and diffusion
- Lateral diffusion limits the proximity between structures



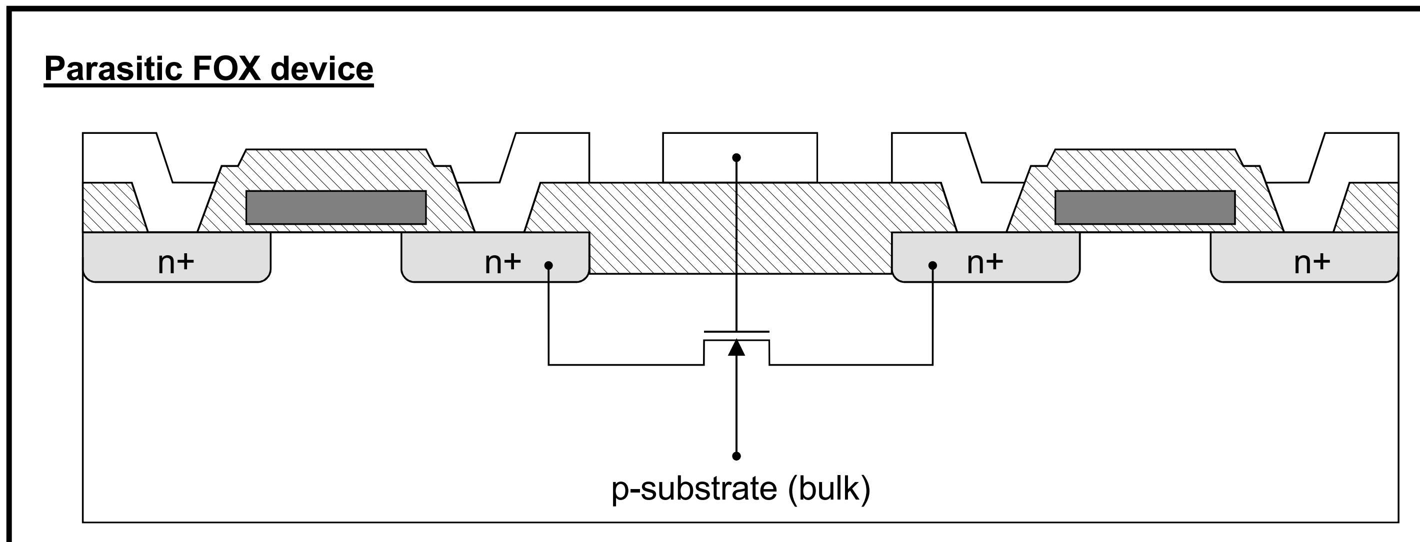
3. Active area definition

- Active area:
  - planar section of the surface where transistors are built
  - defines the gate region (thin oxide)
  - defines the n+ or p+ regions
- A thin layer of SiO_2 is grown over the active region and covered with silicon nitride



4. Isolation

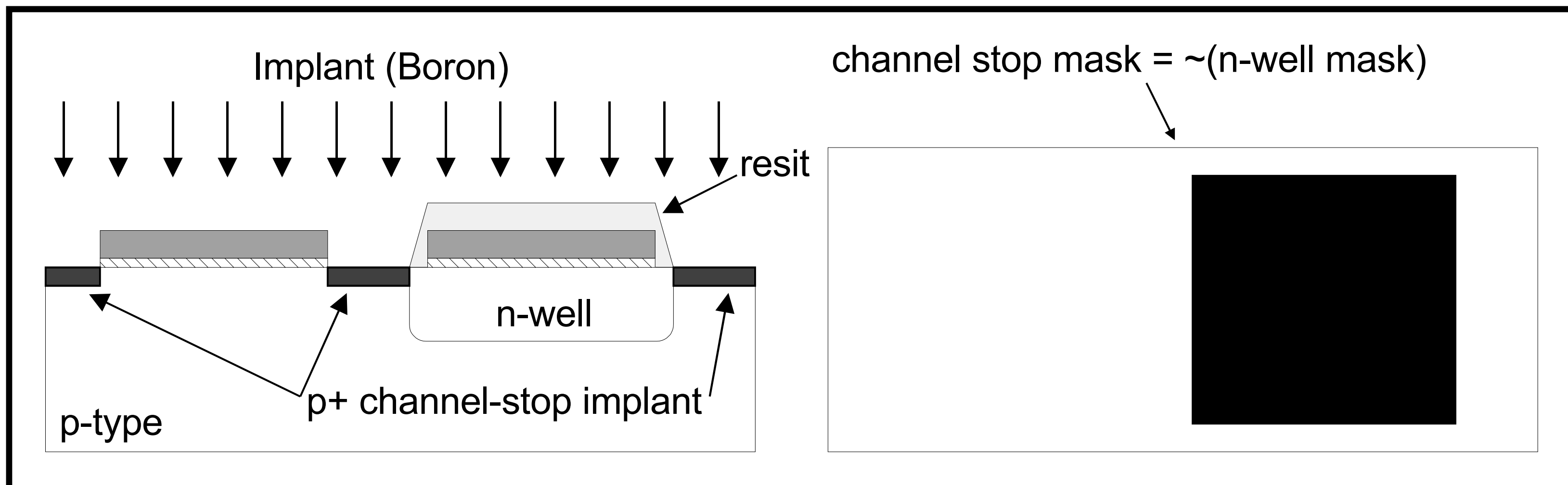
- Parasitic (unwanted) FET's exist between unrelated transistors (Field Oxide FET's)
- Source and drains are existing source and drains of wanted devices
- Gates are metal and polysilicon interconnects
- The threshold voltage of FOX FET's must be higher than Vdd in order to keep them off



4.1 Channel-stop implant

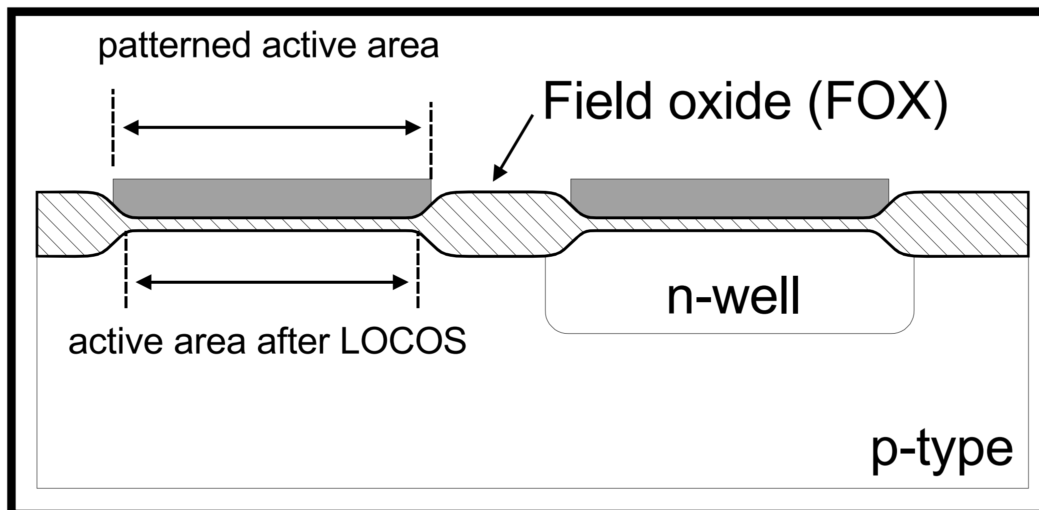
- Increases the threshold voltage by raising the impurity concentration in the substrate in areas where transistors are not required

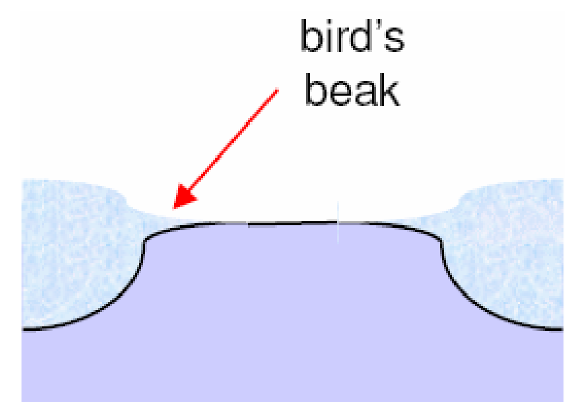
- The silicon nitride (over n-active) and the photoresist (over n-well) act as masks for the channel-stop implant



4.2 Local oxidation of silicon (LOCOS)

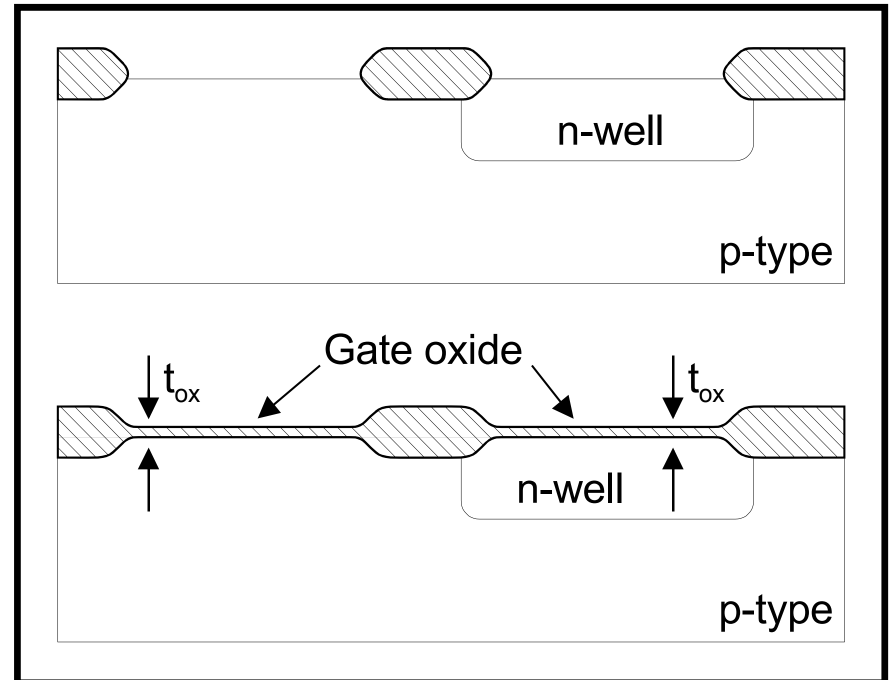
- The photoresist mask is removed
- The SiO_2/Si_3N_4 layers will now act as masks
- Thick silicon dioxide is grown outside the active areas
- This further increases the threshold voltage of parasitic transistors



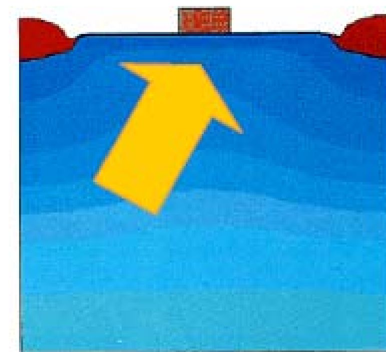


5. Gate oxide growth

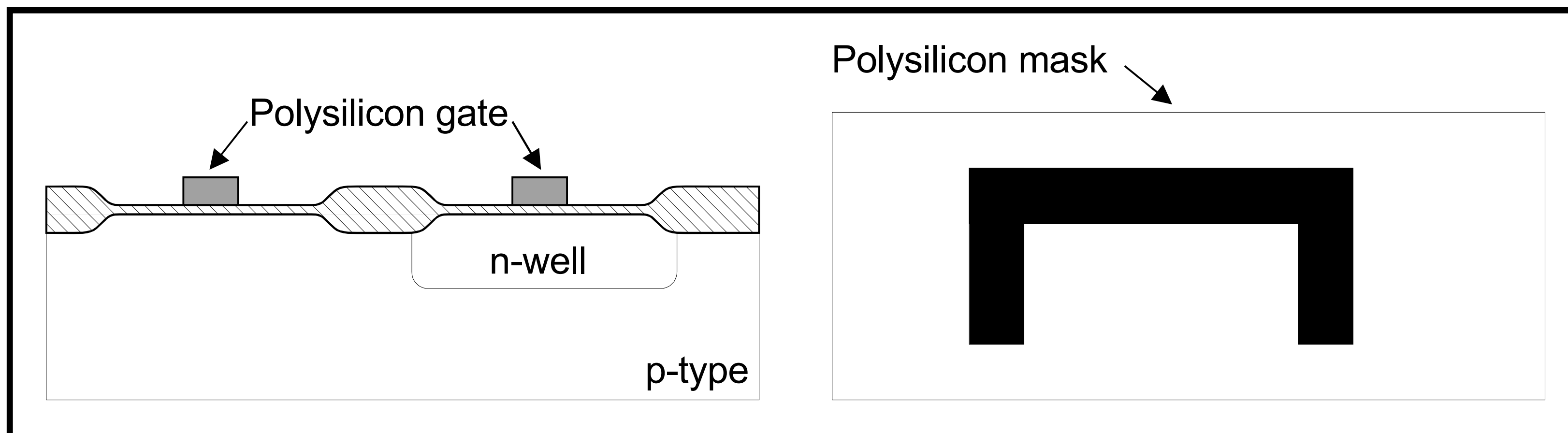
- The nitride and stress-relief oxide are removed
- The devices threshold voltage is adjusted by adding charge at the silicon/oxide interface
- The well controlled gate oxide is grown with thickness t_{ox}



6. Polysilicon deposition and patterning

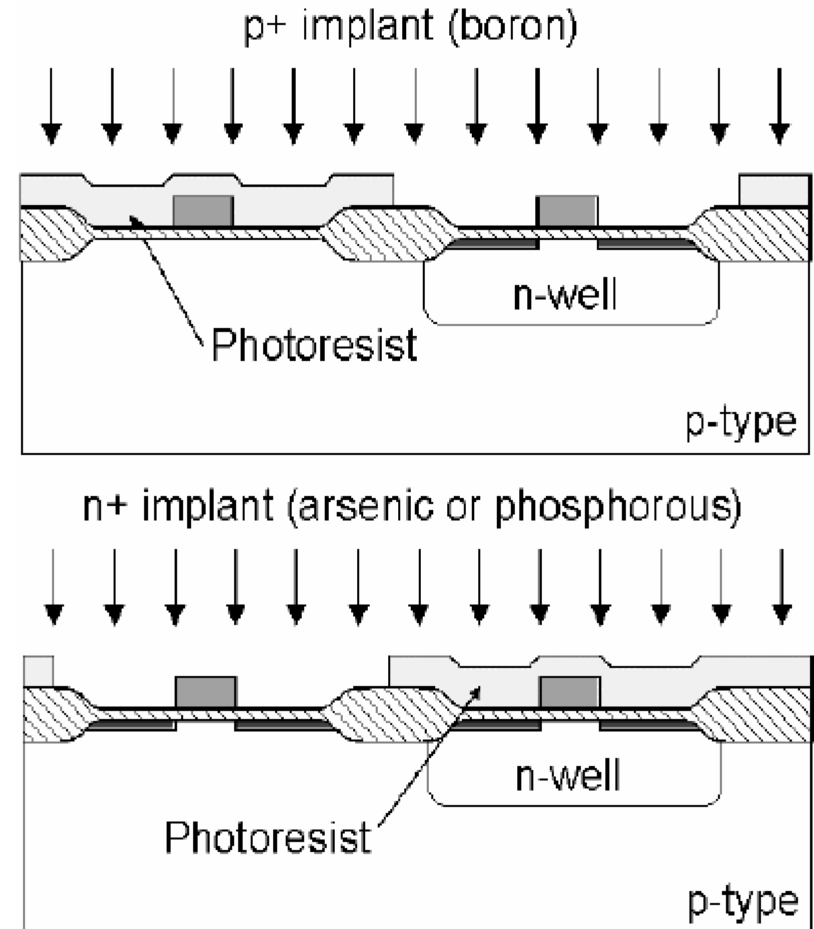


- A layer of polysilicon is deposited over the entire wafer surface
- The polysilicon is then patterned by a lithography sequence
- All the MOSFET gates are defined in a single step
- The polysilicon gate can be doped (n+) while is being deposited to lower its parasitic resistance



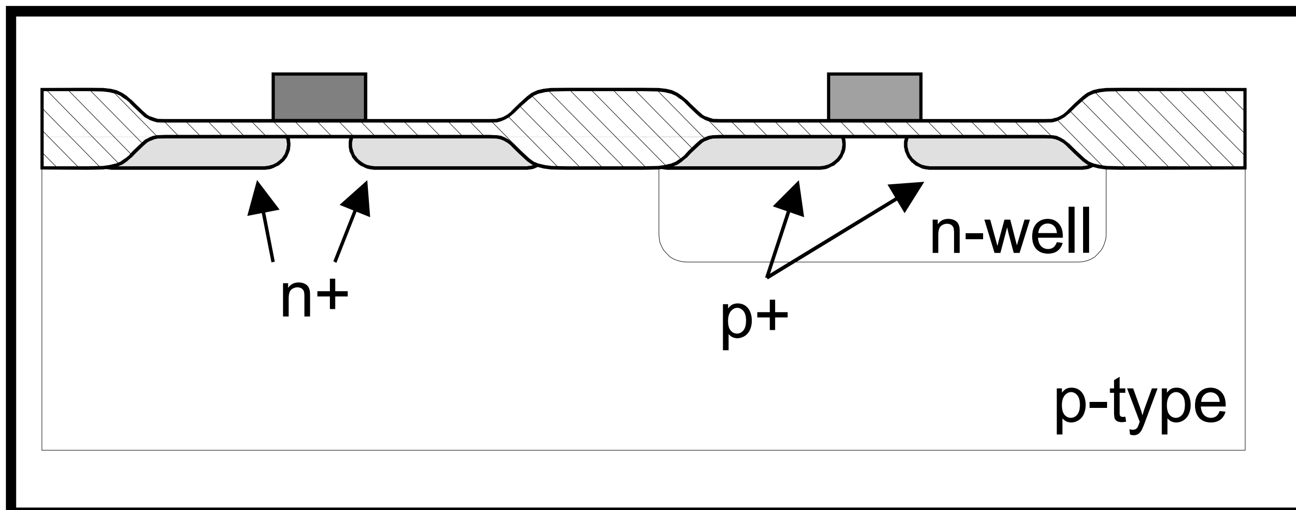
7. Source/Drain Implantation

- Photoresist is patterned to cover all but the desired active area
- The Source and Drain regions of the pMOS or nMOS device are doped by ion implantation
- The polysilicon serves as a mask to the underlying channel



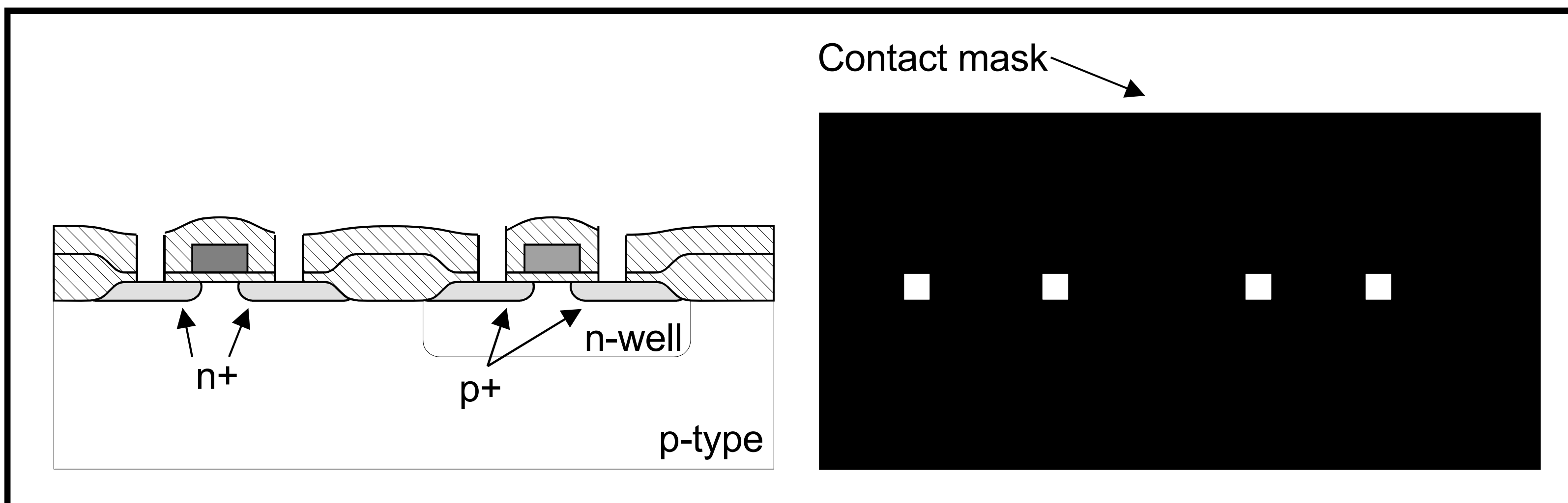
9. Annealing

- After the implants are completed a thermal annealing cycle is executed
- This allows the impurities to diffuse further into the bulk
- The remaining process steps must be kept at as low temperature as possible



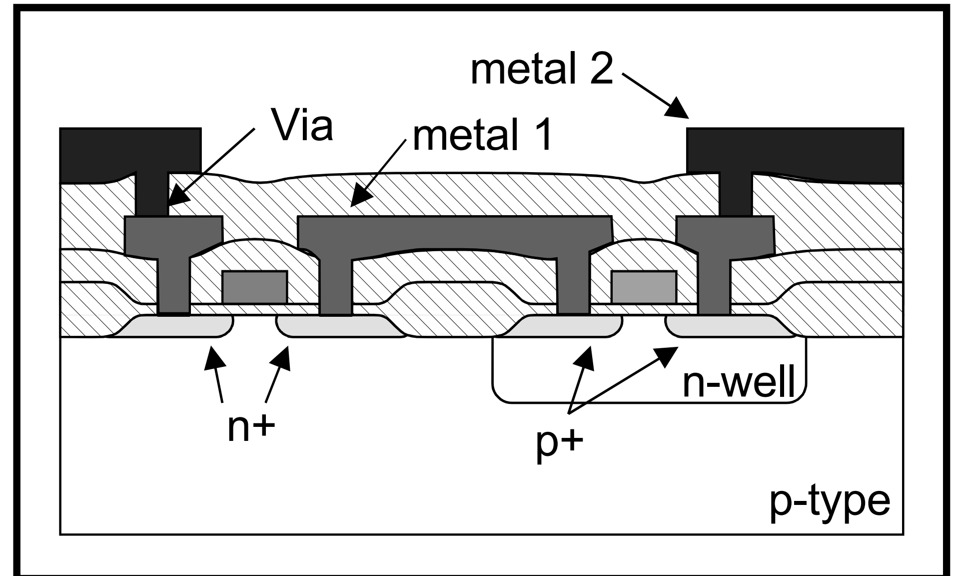
10. Oxide Deposition and Contact Cuts

- The surface of the IC is covered by a layer of field oxide
- Contact cuts are defined by etching SiO_2 down to the surface to be contacted
- These allow metal to contact diffusion and/or polysilicon regions



11. Metallization

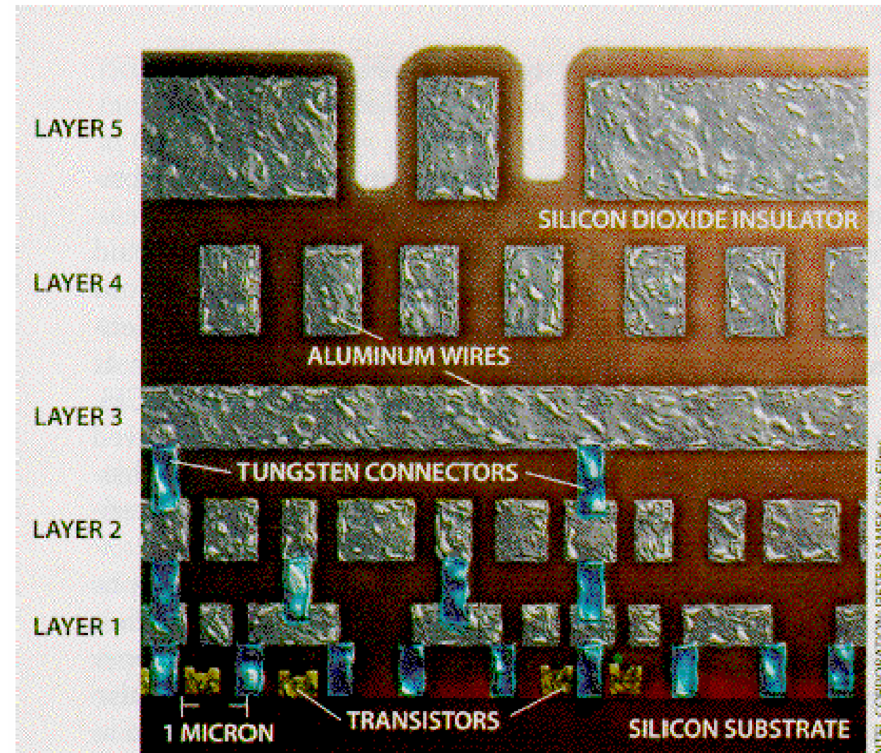
- A first level of metallization is applied to the wafer surface and selectively etched to produce the interconnects
- Another layer of thick oxide is added
- Via openings are created
- Metal 2 is deposited and patterned



- Several other layers of Metal can be added

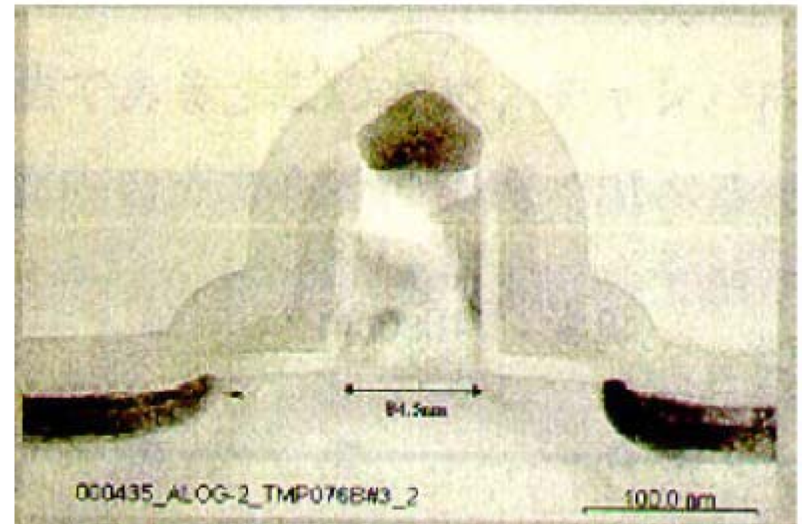
12. Over glass and pad openings

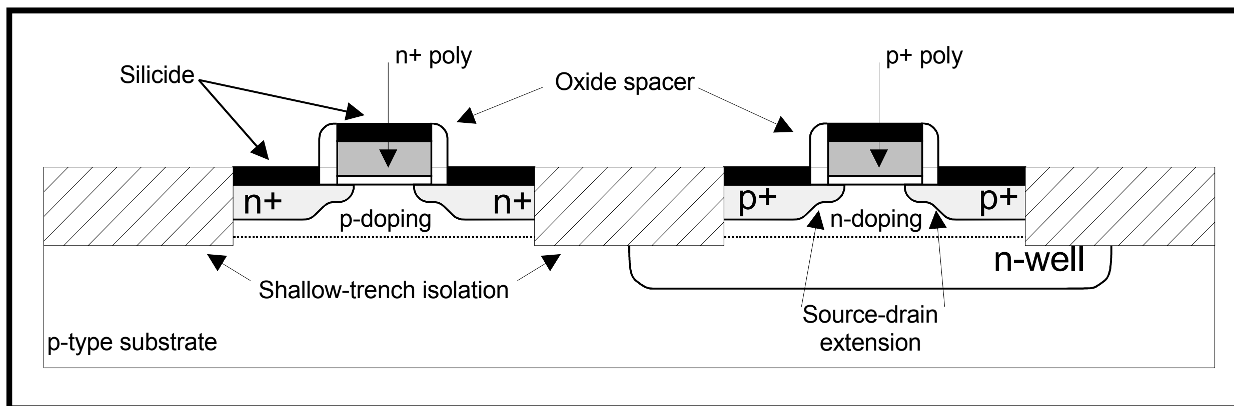
- A protective layer is added over the surface. It consists of:
  - A layer of SiO_2
  - Followed by a layer of silicon nitride
- The SiN layer acts as a diffusion barrier against contaminants (**passivation**)
- Finally, contact cuts are etched to allow for wire bonding

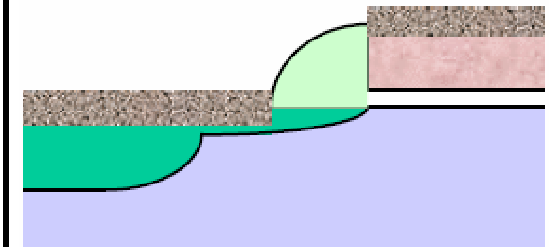


Advanced CMOS processes

- Shallow trench isolation
- source-drain halos (series resistance)
- Self-aligned silicide (spacers)
- …







Links

- http://humanresources.web.cern.ch/Humanresources/ external/training/tech/special/ELEC2002/
  ELEC-2002_11Apr02_3.ppt
- http://lsmwww.epfl.ch/Education/
- http://lsiwww.epfl.ch/LSI2001/teaching/webcourse/toc.html
- www.latticepress.com/prologvol1.html