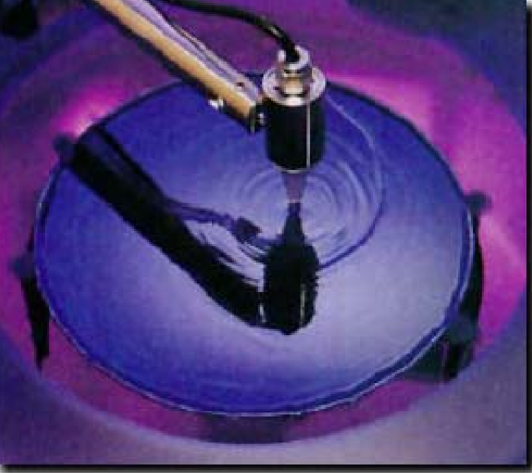


Introduction to VLSI Fabrication Technologies

Emanuele Baravelli

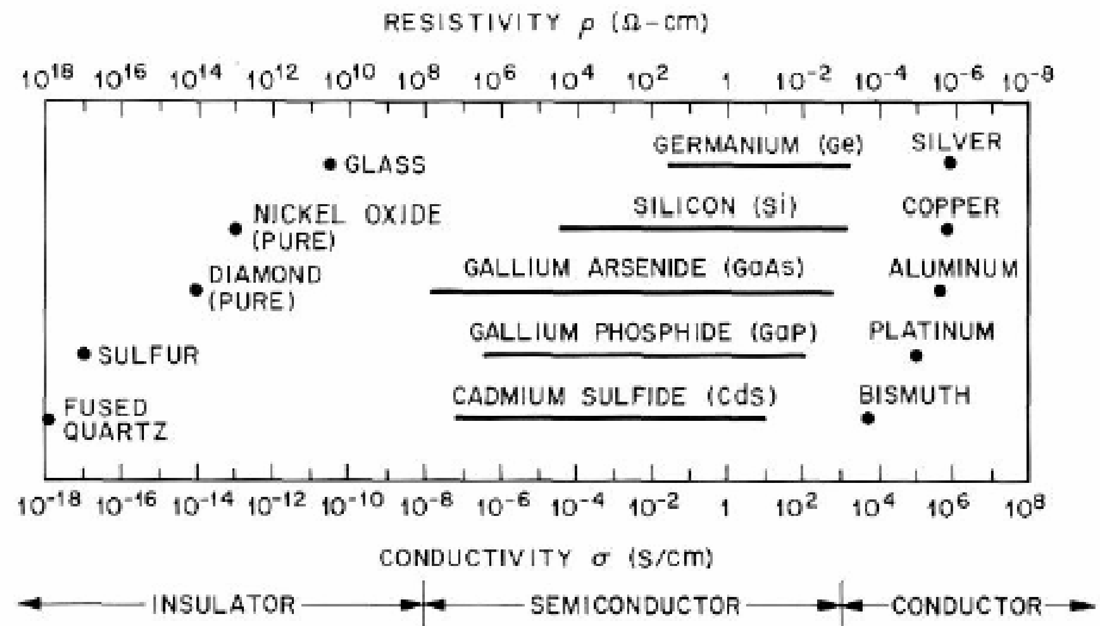
Organization

- Materials Used in VLSI Fabrication
- VLSI Fabrication Technologies
- Overview of Fabrication Methods
- Device simulation

Main Categories of Materials

Materials can be classified into three main groups regarding their electrical conduction properties:

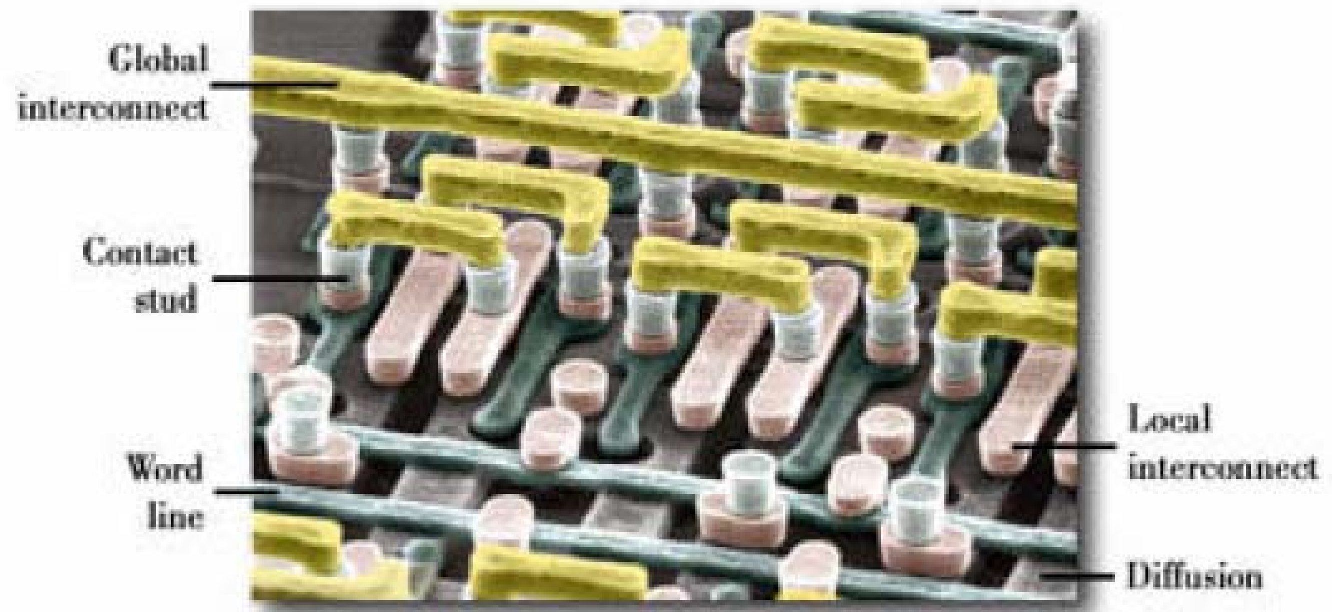
- **Insulators**
- **Conductors**
- **Semiconductors**



Conductors

Conductors are used in IC design for electrical connectivity. The following are good conducting elements:

- **Silver**
- **Gold**
- **Copper**
- **Aluminum**
- **Platinum**



Insulators

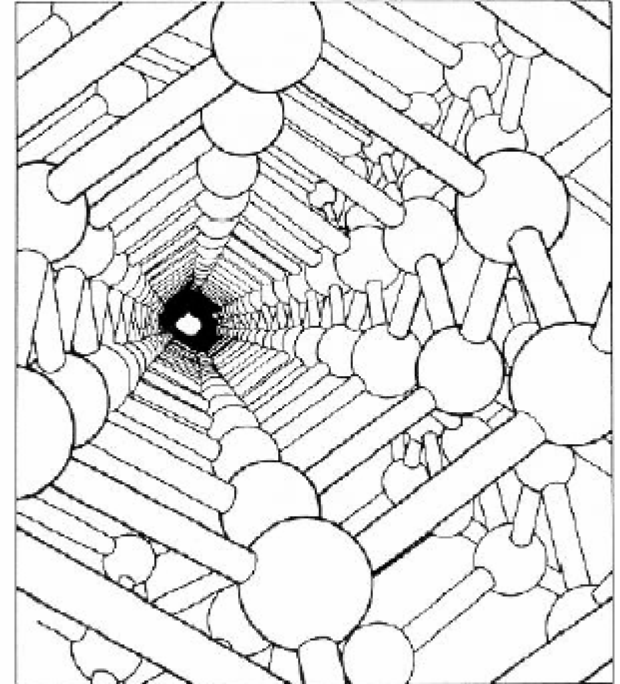
Insulators are used to isolate conducting and/or semi-conducting materials from each other.

MOS devices and Capacitors rely on an insulator for their physical operation.

The choice of the insulators (and the conductors) in IC design depends heavily on how the materials interact with each other, especially with the semiconductors.

Semiconductors

- The basic semiconductor material used in device fabrication is **Silicon**
- The success of this material is due to:
  - Phisical characteristics
  - Abundance in nature and very low cost
  - Relatively easy process
  - Reliable high volume fabrication



- Other semiconductors (e.g. GaAs) are used for special applications

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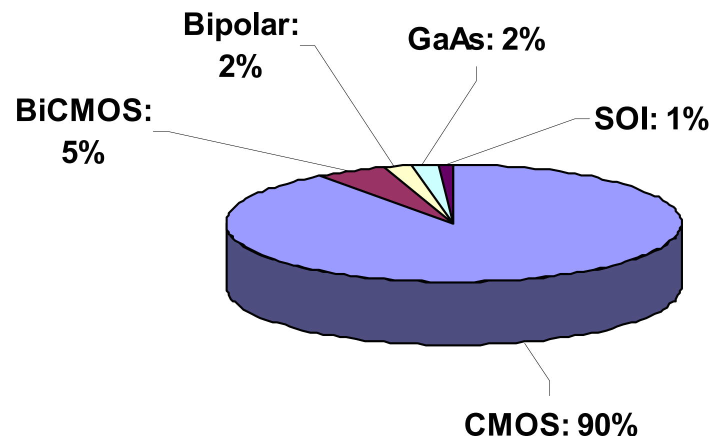
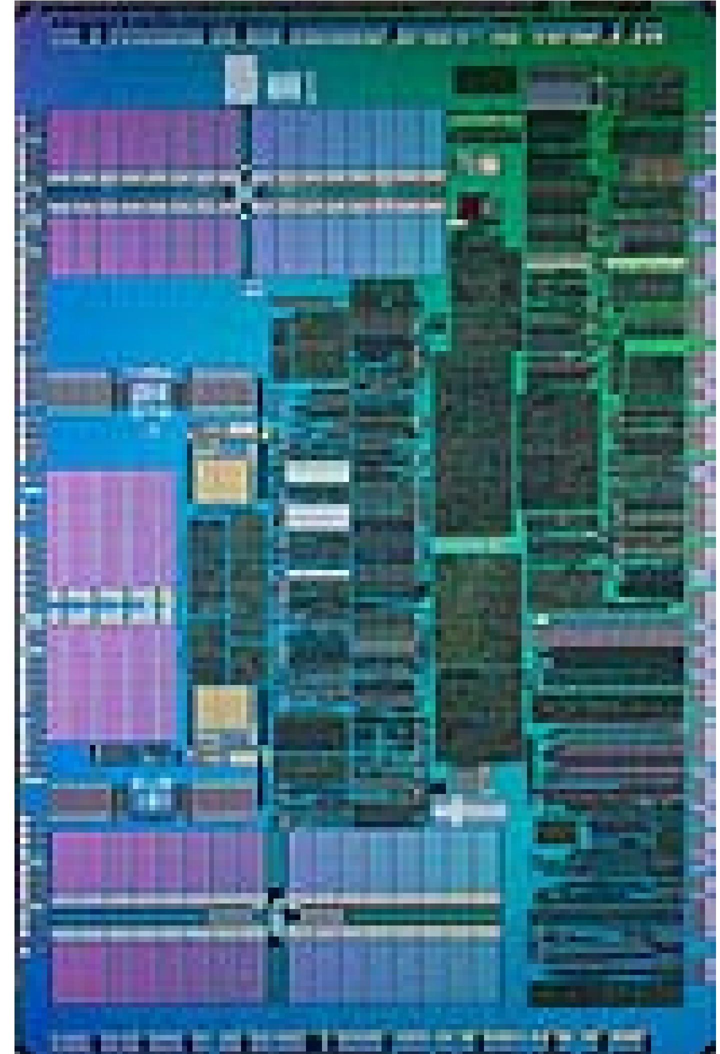
Overview of Processing Technologies

Although a number of processing technologies are available, the majority of the production is done with traditional CMOS. Other processes are limited to areas where CMOS is not very suitable (like high speed RF applications)

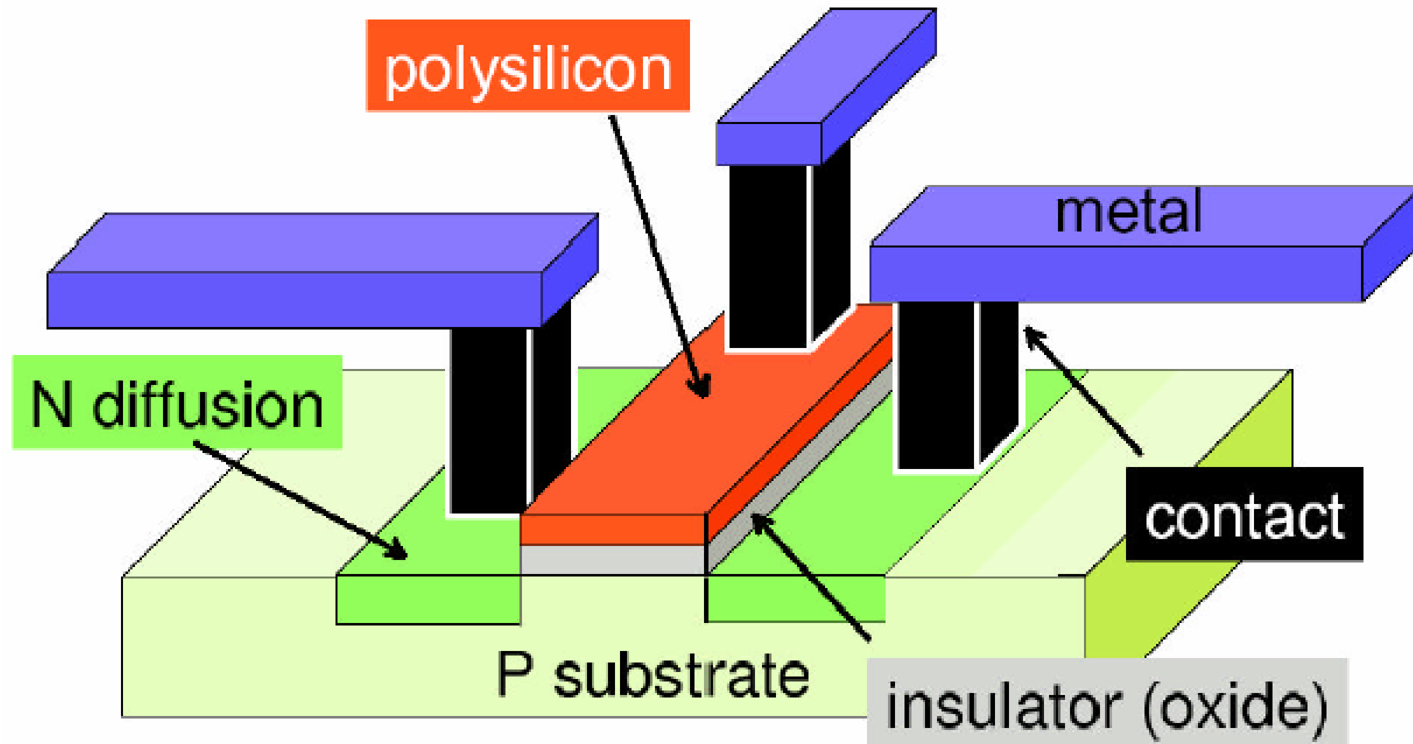


CMOS technology

- An **Integrated Circuit (IC)** is an electronic network fabricated in a single piece of a semiconductor material
- The semiconductor surface is subjected to various processing steps in which impurities and other materials are added with specific geometrical patterns
- The fabrication steps are sequenced to form three dimensional regions that act as transistors and interconnects that form the network

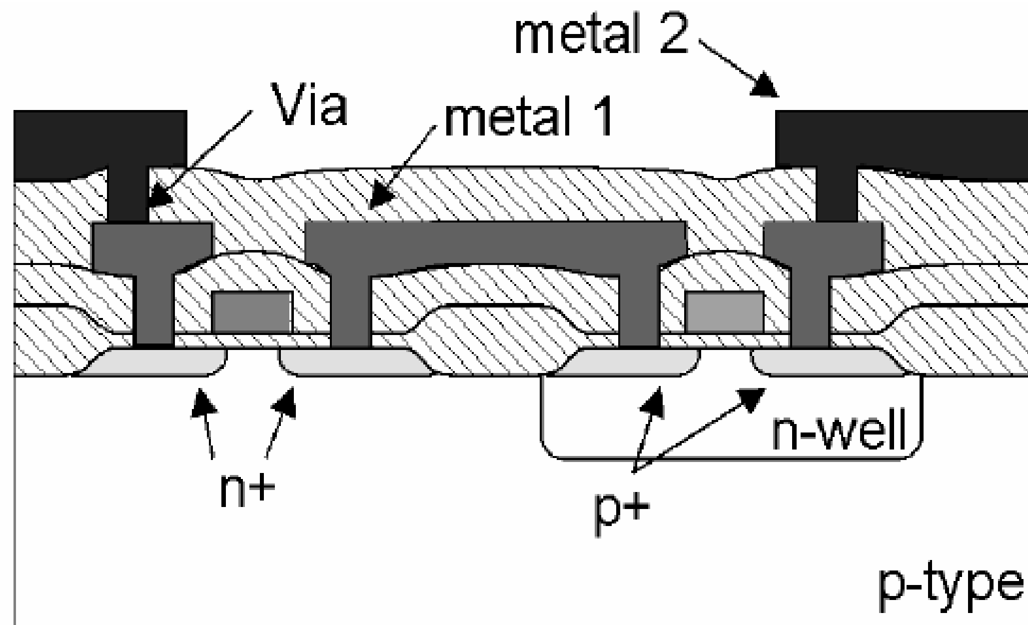


Simplified View of MOSFET



CMOS Process

The CMOS process allows fabrication of nMOS and pMOS transistors side-by-side on the same Silicon substrate.



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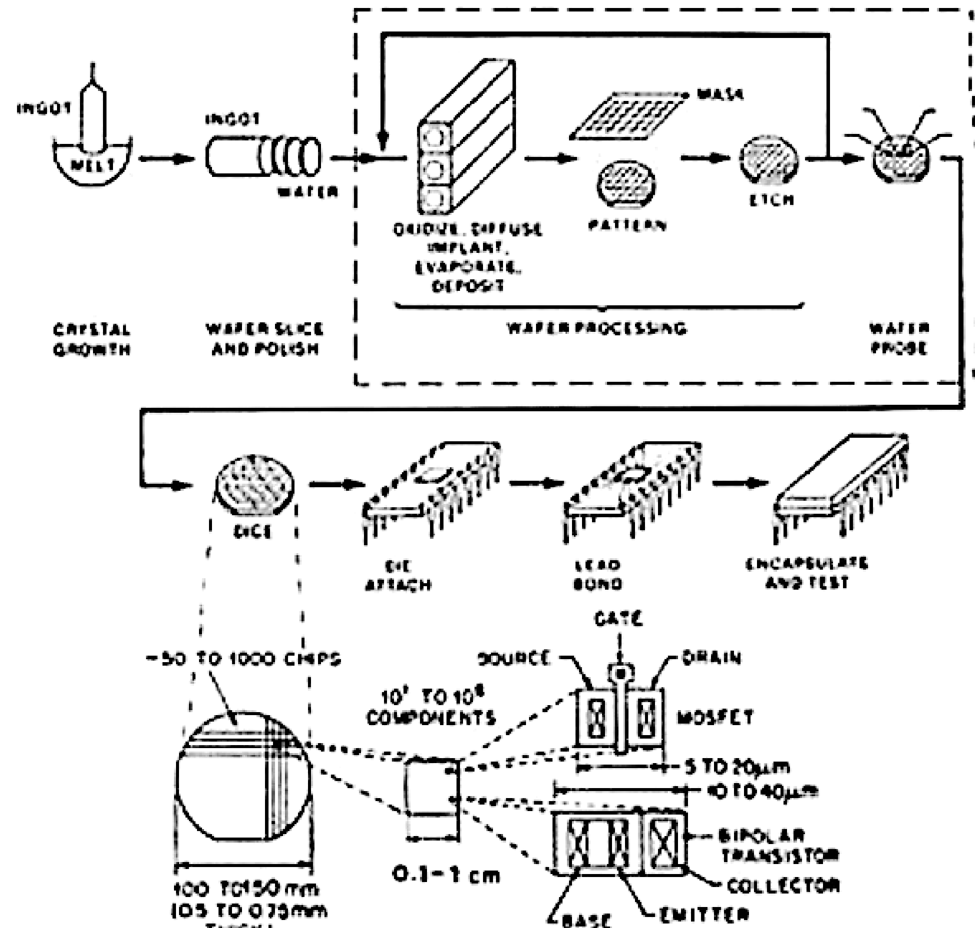
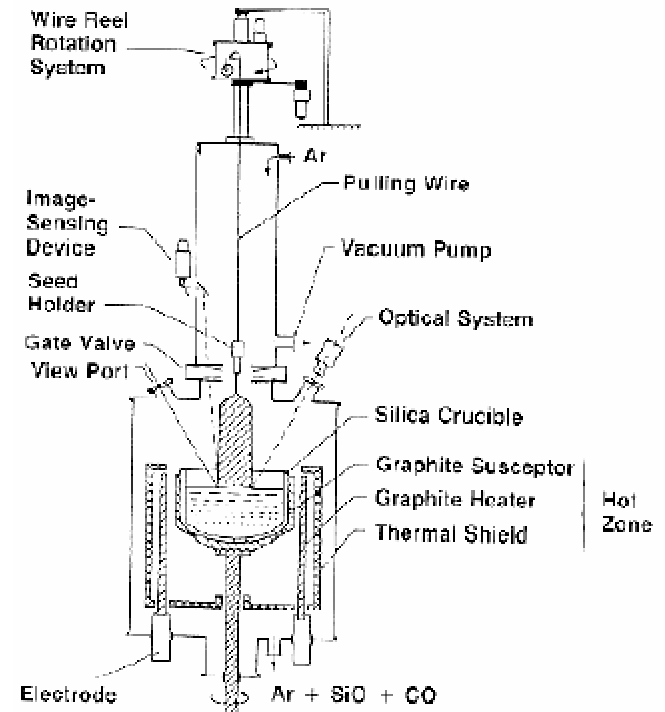
Fabrication process sequence

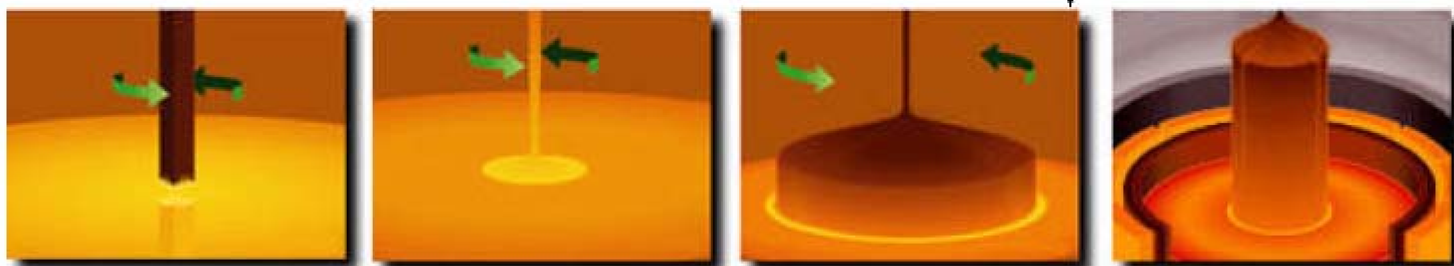
- Silicon manifacture
- Wafer processing
  - Lithography
  - Oxide growth and removal
  - Diffusion and ion implantation
  - Annealing
  - Silicon deposition
  - Metallization
- Testing
- Assembly and packaging



Single Crystal Growth (I)

- Pure silicon is melted in a pot (1400° C) and a small seed containing the desired crystal orientation is inserted into molten silicon and slowly (1mm/minute) pulled out.



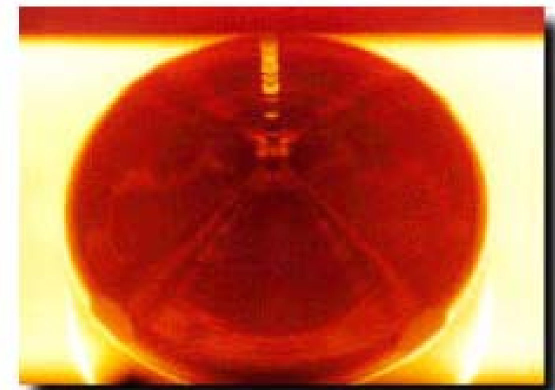


Single Crystal Growth (II)

- The silicon crystal (in some cases also containing doping) is manufactured as a cylinder (**ingot**) with a diameter of 8-12 inches (1”=2.54 cm).

Single Crystal Silicon Ingot

- This cylinder is carefully sawed into thin (0.50-0.75 mm thick) disks called **wafers**, which are later polished and marked for crystal orientation.



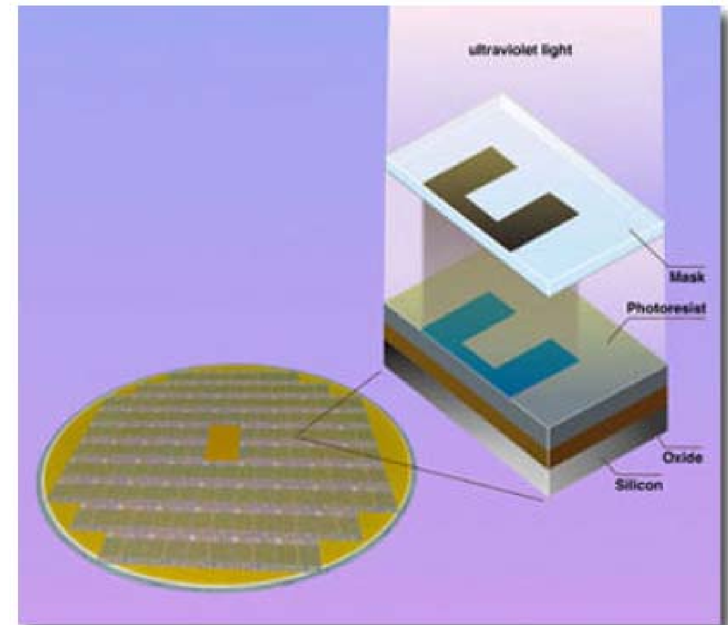
Inside CZ Puller
(MEMC)

Lithography (I)

Lithography: process used to transfer patterns to each layer of the IC

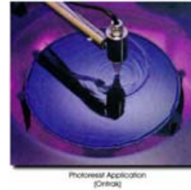
Lithography sequence steps:

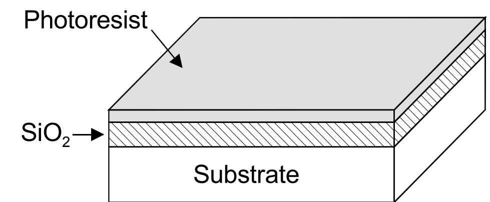
- <u>Designer</u>:
  - Drawing the "layer" patterns on a layout editor
- <u>Silicon Foundry</u>:
  - Masks generation from the layer patterns in the design data base
  - Printing: transfer the mask pattern to the wafer surface
  - Process the wafer to physically pattern each layer of the IC



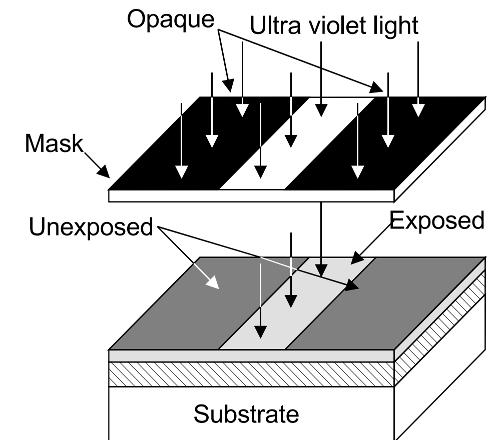
Lithography (II)

1. Photoresist application:
   - the surface to be patterned is spin-coated with a light-sensitive organic polymer called photoresist

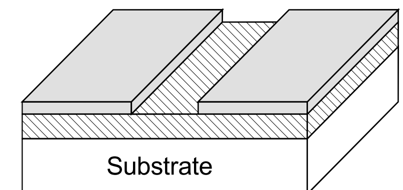




2. Printing (exposure):
   - the mask pattern is developed on the photoresist, with UV light exposure
   - depending on the type of photoresist (negative or positive), the exposed or unexposed parts become resistant to certain types of solvents



3. Development:
   - the soluble photoresist is chemically removed
   - The developed photoresist acts as a mask for patterning of underlying layers and then is removed.

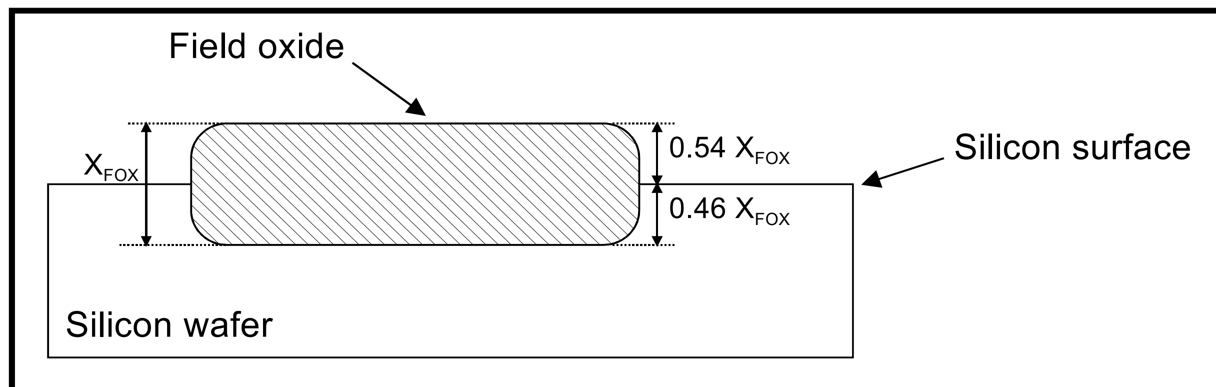


Oxide Growth / Oxide Deposition

- Oxide can be **grown** from silicon through heating in an oxidizing atmosphere
  - Gate oxide, device isolation
  - Oxidation consumes silicon

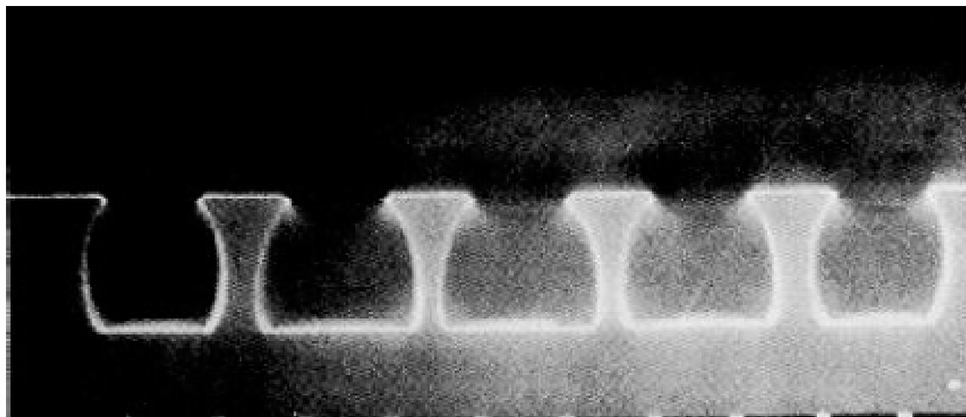
Oxidation Furnace
(Silicon Valley Group - Thermco Systems)

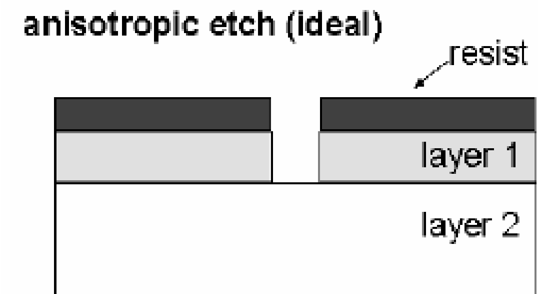
- SiO_2 is **deposited** on materials other than silicon through reaction between gaseous silicon compounds and oxidizers
  - Insulation between different layers of metallization

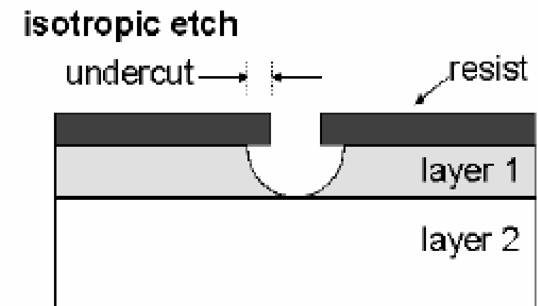


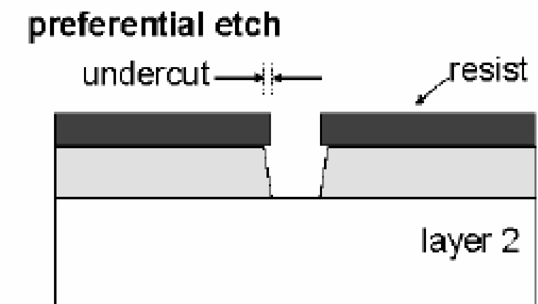
Etching

- Once the desired shape is patterned with photoresist, the **etching** process allows unprotected materials to be removed
  - Wet etching: uses chemicals
  - Dry or plasma etching: uses ionized gases





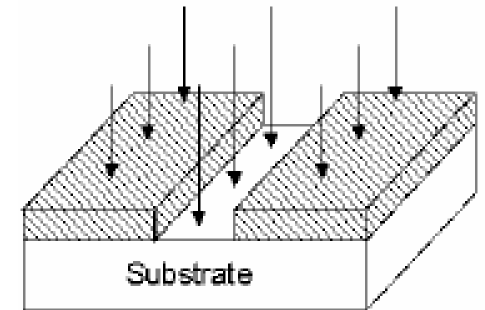


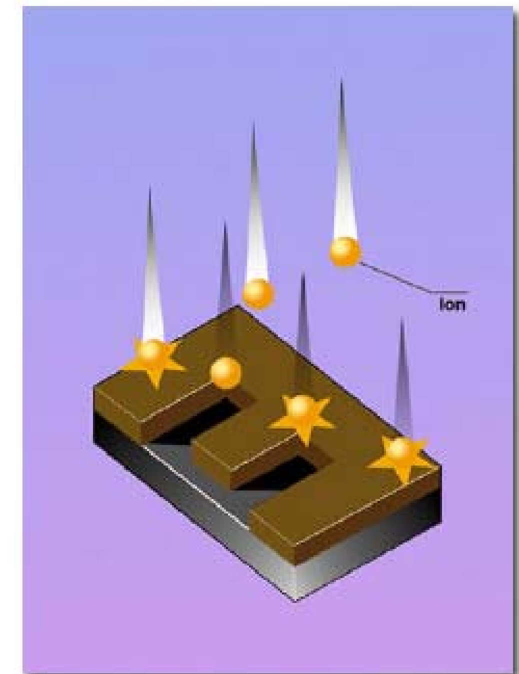


Diffusion and Ion Implantation

Doping materials are added to change the electrical characteristics of silicon locally through:

- **Diffusion**: dopants deposited on silicon move through the lattice by thermal diffusion (high temperature process)
  - Wells
- **Ion implantation**: highly energized donor or acceptor atoms impinge on the surface and travel below it
  - The patterned SiO_2 serves as an implantation mask
  - Source and Drain regions





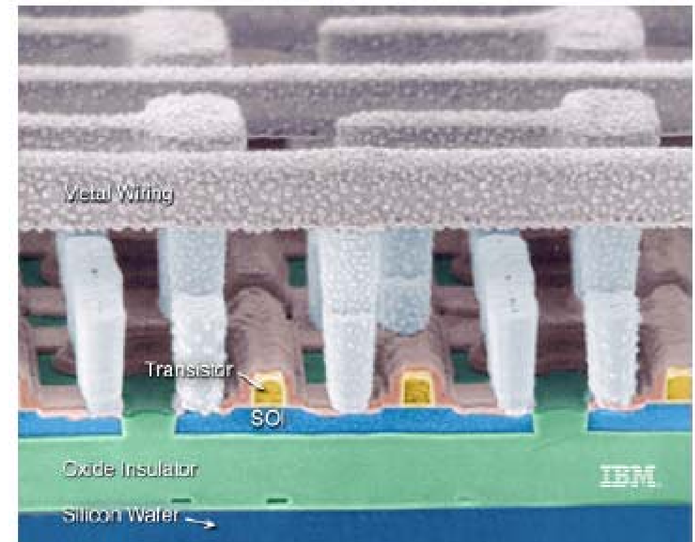
Annealing

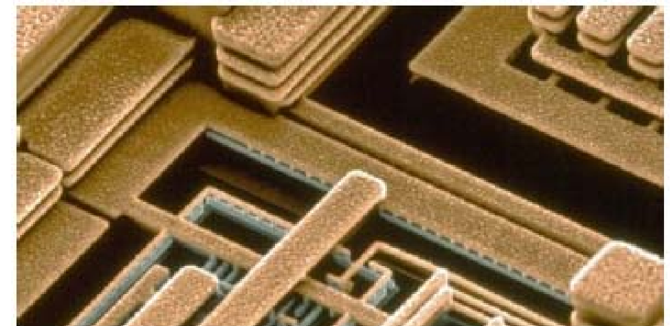
Thermal annealing is a high temperature process which:

- allows doping impurities to diffuse further into the bulk
- repairs lattice damage caused by the collisions with doping ions

Silicon Deposition and Metallization

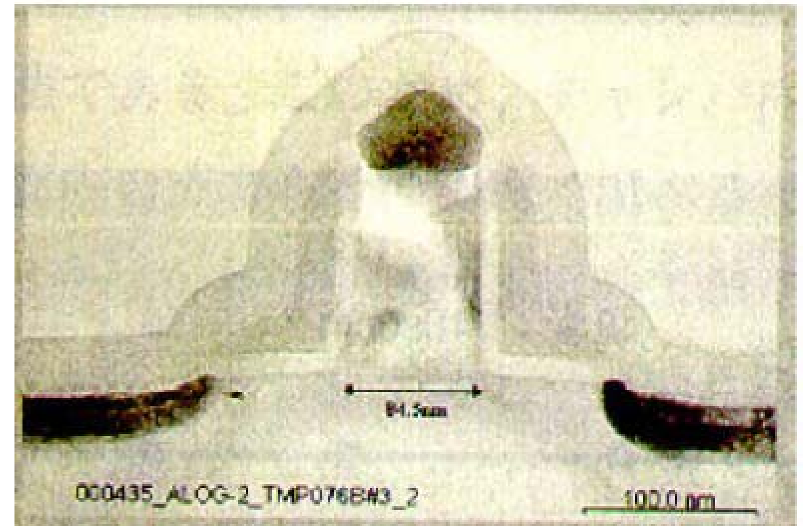
- Films of silicon can be added on the surface of a wafer
  - **Epitaxy**: growth of a single-crystal semiconductor film on a crystalline substate
  - **Polysilicon**: polycrystalline film with a granular structure obtained through deposition of silicon on an amorphous material
    - MOSFET gates
- Metallization: deposition of metal layers by evaporation
  - interconnections

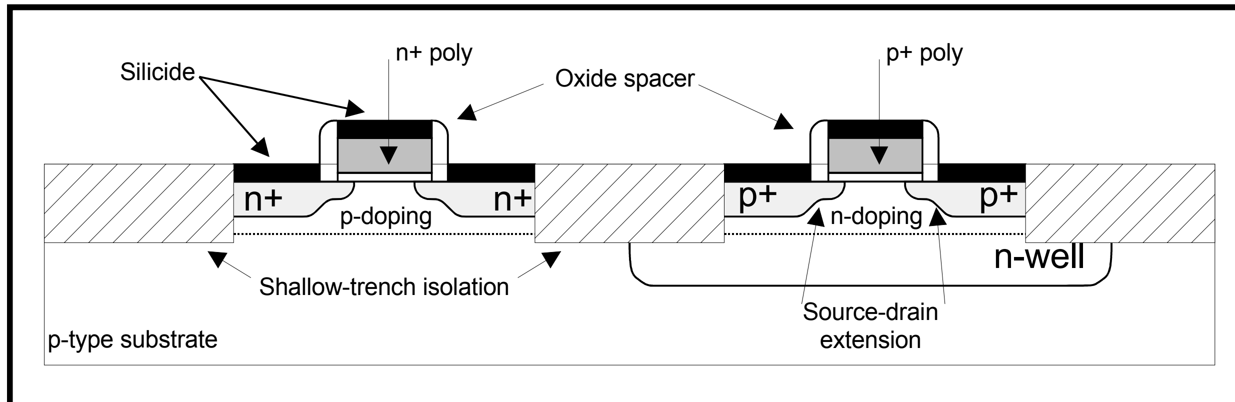


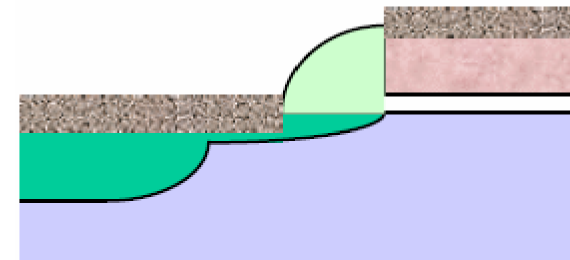


Advanced CMOS processes

- Shallow trench isolation
- source-drain halos (series resistance)
- Self-aligned silicide (spacers)
- …







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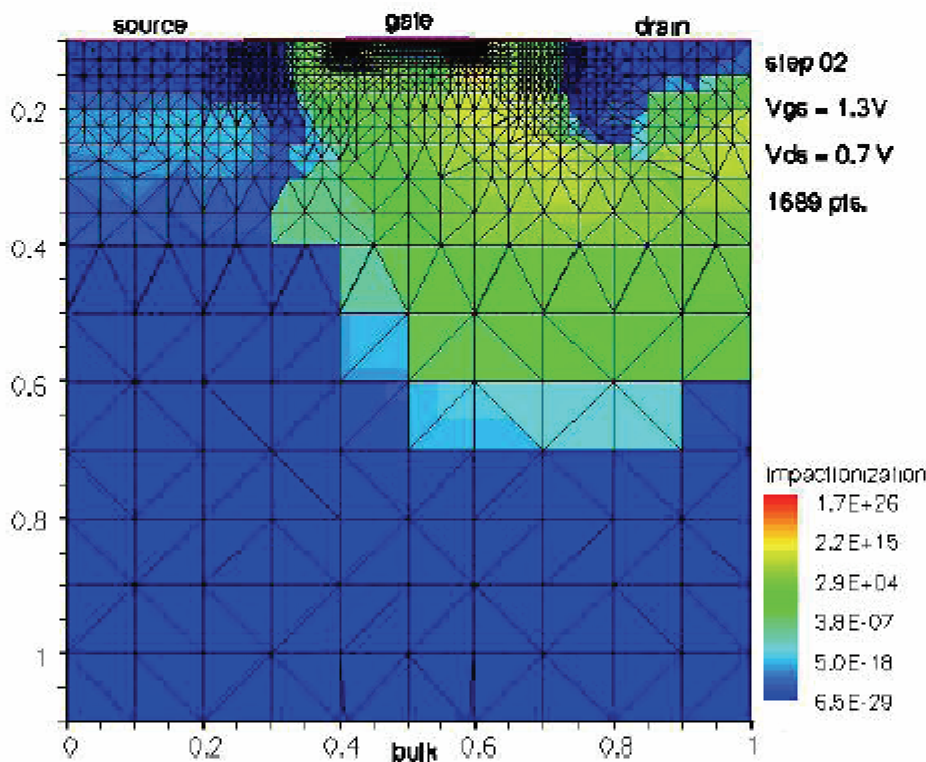
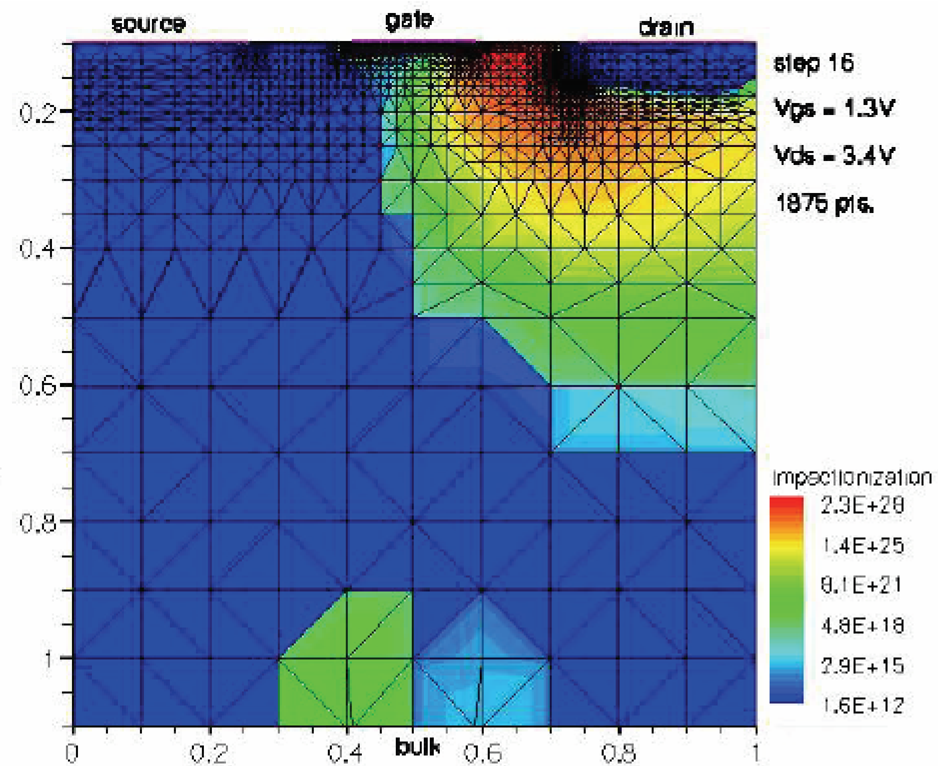
MOS device simulation

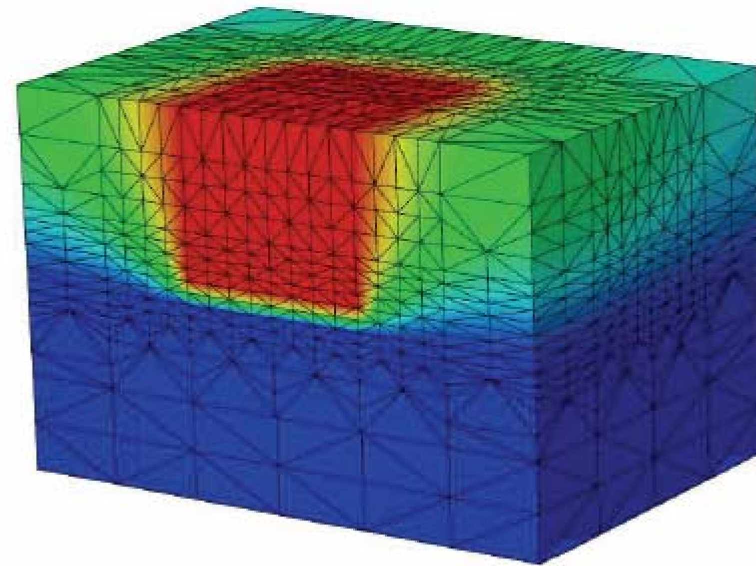
- 2D 0.18 μm n-channel MOS, tox = 4 nm
- Id (Vds) simulation, Vgs=1.3V
- 8 refinement cycles
- Refinement on *ψ*, *n* , *p*

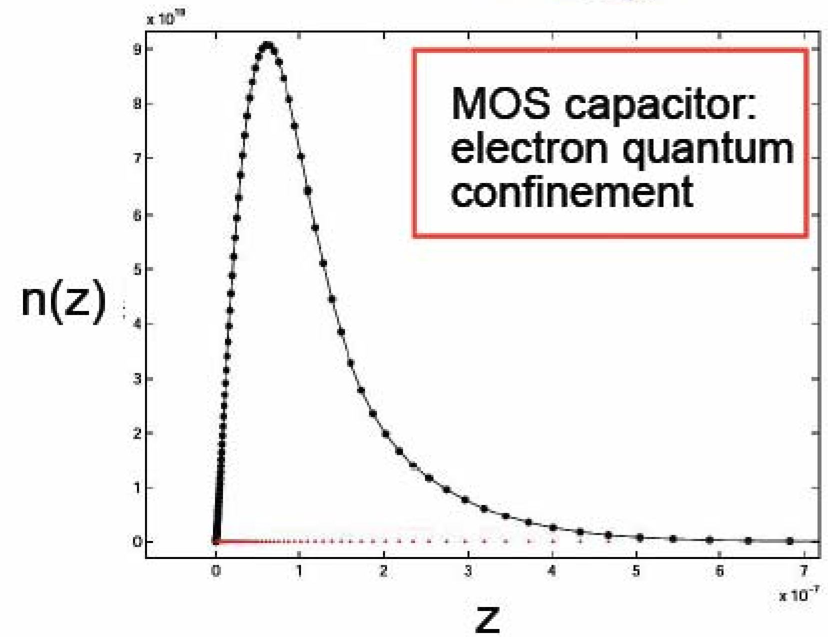




Research activities

- Geometrical issues:
  - Sophisticated 2D geometries
    (2nd generation wavelets)
  - 3D geometries
- Simulation issues:
  - Advanced models (hydrodynamic, quantum effects)





Links

- http://humanresources.web.cern.ch/Humanresources/external/training/tech/special/ELEC2002/ELEC-2002_11Apr02_3.ppt
- http://lsmwww.epfl.ch/Education/
- http://lsiwww.epfl.ch/LSI2001/teaching/webcourse/toc.html
- www.latticepress.com/prologvol1.html