.AC (AC Analysis)

Purpose The .AC command calculates the frequency response of a circuit over a range of frequencies.

General Form

```
.AC <sweep type> <points value>
+ <start frequency value> <end frequency value>
```

Examples

```
.AC LIN 101 100Hz  200Hz
.AC OCT  10  1kHz  16kHz
.AC DEC  20  1MEG 100MEG
```

Arguments and Options

<sweep type>
Must be LIN, OCT, or DEC, as described below.

Parameter	Description	Description
LIN	linear sweep	The frequency is swept linearly from the starting to the ending frequency. The <points value> is the total number of points in the sweep.
OCT	sweep by octaves	The frequency is swept logarithmically by octaves. The <points value> is the number of points per octave.
DEC	sweep by decades	The frequency is swept logarithmically by decades. The <points value> is the number of points per decade.

<points value>
Specifies the number of points in the sweep, using an integer.

<start frequency value> <end frequency value>
The end frequency value must not be less than the start frequency value, and both must be greater than zero. The whole sweep must include at least one point. If a group delay (G suffix) is specified as an output, the frequency steps must be close enough together that the phase of that output changes smoothly from one frequency to the next. Calculate group delay by subtracting the phases of successive outputs and dividing by the frequency increment.

Comments A **.PRINT (Print)**, **.PLOT (Plot)**, or **.PROBE (Probe)** command must be used to get the results of the AC sweep analysis.

AC analysis is a linear analysis. The simulator calculates the frequency response by linearizing the circuit around the bias point.

All independent voltage and current sources that have AC values are inputs to the circuit. During AC analysis, the only independent sources that have nonzero amplitudes are those using AC specifications. The SIN specification does not count, as it is used only during transient analysis.

To analyze nonlinear functions such as mixers, frequency doublers, and AGC, use **.TRAN (Transient Analysis)**.

Chapter

.DC (DC Analysis)

Purpose

The .DC command performs a linear, logarithmic, or nested DC sweep analysis on the circuit. The DC sweep analysis calculates the circuit's bias point over a range of values for <sweep variable name>.

Sweep Type

The sweep can be linear, logarithmic, or a list of values.

Parameter	Description	Meaning
LIN	linear sweep	The sweep variable is swept linearly from the starting to the ending value.
OCT	sweep by octaves	Sweep by octaves. The sweep variable is swept logarithmically by octaves.
DEC	sweep by decades	Sweep by decades. The sweep variable is swept logarithmically by decades.
LIST	list of values	Use a list of values.

Chapter

Linear Sweep

General Form

```
.DC [LIN] <sweep variable name>
+ <start value> <end value> <increment value>
+ [nested sweep specification]
```

Examples

```
.DC VIN -.25  .25  .05
.DC LIN I2  5mA  -2mA  0.1mA
.DC VCE 0V 10V .5V  IB 0mA 1mA 50uA
.DC RES RMOD(R)  0.9  1.1  .001
```

Arguments and Options

<start value>
Can be greater or less than <end value>: that is, the sweep can go in either direction.

<increment value>
The step size. This value must be greater than zero.

Comments

The sweep variable is swept linearly from the starting to the ending value.

The keyword LIN is optional.

Logarithmic Sweep

General Form

```
.DC <logarithmic sweep type> <sweep variable name>
+ <start value> <end value> <points value>
+ [nested sweep specification]
```

Examples

```
.DC DEC NPN QFAST(IS) 1E-18 1E-14  5
```

Arguments and Options

<logarithmic sweep type>
Must be specified as either DEC (to sweep by decades) or OCT (to sweep by octaves).

<start value>
Must be positive and less than <end value>.

<points value>
The number of steps per octave or per decade in the sweep. This value must be an integer.

Comments

Either `OCT` or `DEC` must be specified for the <logarithmic sweep type>.

Nested Sweep

General Form

```
.DC <sweep variable name> LIST <value>*
+[nested sweep specification]
```

Examples

```
.DC TEMP LIST 0 20 27 50 80 100 PARAM Vsupply 7.5 15 .5
```

Arguments and Options

<sweep variable name>

After the DC sweep is finished, the value associated with <sweep variable name> is set back to the value it had before the sweep started. The following items can be used as sweep variables in a DC sweep:

Parameter	Description	Meaning
Source	A name of an independent voltage or current source.	During the sweep, the source's voltage or current is set to the sweep value.
Model Parameter	A model type and model name followed by a model parameter name in parenthesis.	The parameter in the model is set to the sweep value. The following model parameters cannot be (usefully) swept: L and W for the MOSFET device (use LD and WD as a work around), and any temperature parameters, such as TC1 and TC2 for the resistor.
Temperature	Use the keyword TEMP for <sweep variable name>.	Set the temperature to the sweep value. For each value in the sweep, all the circuit components have their model parameters updated to that temperature.
Global Parameter	Use the keyword PARAM, followed by the parameter name, for <sweep variable name>.	During the sweep, the global parameter's value is set to the sweep value and all expressions are reevaluated.

Comments

For a nested sweep, a second sweep variable, sweep type, start, end, and increment values can be placed after the first sweep. In the nested sweep example, the first sweep is the inner loop: the entire first sweep is performed for each value of the second sweep.

When using a list of values, there are no start and end values. Instead, the numbers that follow the keyword LIST are the values that the sweep variable is set to.

The rules for the values in the second sweep are the same as for the first. The second sweep generates an entire **.PRINT (Print)** table or **.PLOT (Plot)** plot for each value of the sweep. Probe displays nested sweeps as a family of curves.

Section

.END (End of Circuit)

Purpose

The .END command marks the end of the circuit. All the data and every other command must come before it. When the .END command is reached, PSpice does all the specified analyses on the circuit.

General Form

```
.END
```

Examples

```
* 1st circuit in file
... circuit definition
.END
* 2nd circuit in file
... circuit definition
.END
```

Comments

There can be more than one circuit in an input file. Each circuit is marked by an .END command. PSpice processes all the analyses for each circuit before going on to the next one.

Everything is reset at the beginning of each circuit. Having several circuits in one file gives the same results as having them in separate files and running each one separately. However, all the simulation results go into one `.OUT` file and one `.DAT` file. This is a convenient way to arrange a set of runs for overnight operation.

The last statement in an input file must be an .END command.

Chapter

.MODEL (Model)

Purpose

The .MODEL command defines a set of device parameters which can be referenced by devices in the circuit.

General Form

```
.MODEL <model name> [AKO: <reference model name>]
+ <model type>
+ ([<parameter name> = <value> [tolerance specification]]*
+ [T_MEASURED=<value>] [[T_ABS=<value>] or
+ [T_REL_GLOBAL=<value>] or [T_REL_LOCAL=<value>]])
```

Examples

```
.MODEL RMAX RES (R=1.5 TC1=.02 TC2=.005)
.MODEL DNOM D (IS=1E-9)
.MODEL QDRIV NPN (IS=1E-7 BF=30)
.MODEL MLOAD NMOS(LEVEL=1 VTO=.7 CJ=.02pF)
.MODEL CMOD CAP (C=1 DEV 5%)
.MODEL DLOAD D (IS=1E-9 DEV .5% LOT 10%)
.MODEL RTRACK RES (R=1 DEV/GAUSS 1% LOT/UNIFORM 5%)
.MODEL QDR2 AKO:QDRIV NPN (BF=50 IKF=50m)
```

Arguments and Options

<model name>

The model name which is used to reference a particular model.

<reference model name>

The model types of the current model and the AKO (A Kind Of) reference model must be the same. The value of each parameter of the referenced model is used unless overridden by the current model, e.g., for QDR2 in the last example, the value of IS derives from QDRIV, but the values of BF and IKF come from the current definition. Parameter values or formulas are transferred, but not the tolerance specification. The referenced model can be in the main circuit file, accessed through a .INC command, or it can be in a library file; see **.LIB (Library File)**.

<model type>

Must be one of the types outlined in the table that follows.

Devices can only reference models of a corresponding type; for example:

- A JFET can reference a model of types NJF or PJF, but not of type NPN.
- There can be more than one model of the same type in a circuit, although they must have different names.

Following the <model type> is a list of parameter values enclosed by parentheses. None, any, or all of the parameters can be assigned values. Default values are used for all unassigned parameters. The lists of parameter names, meanings, and default values are found in the individual device descriptions.

Chapter

.OP (Bias Point)

Purpose

The .OP command causes detailed information about the bias point to be printed.

General Form

```
.OP
```

Examples

```
.OP
```

Comments

This command does not write output to the Probe data file. The bias point is calculated regardless of whether there is a .OP command. Without the .OP command, the only information about the bias point in the output is a list of the node voltages, voltage source currents, and total power dissipation.

Using a .OP command can cause the small-signal (linearized) parameters of all the nonlinear controlled sources and all the semiconductor devices to be printed in the output file.

The .OP command controls the output for the regular bias point only. The **.TRAN (Transient Analysis)** command controls the output for the transient analysis bias point.

If no other analysis is performed, then no Probe data file is created.

Chapter

If the different output variables differ considerably in their output ranges, then the plot is given more than one y-axis using ranges corresponding to the different output variables.

The y-axis of frequency response plots (AC) is always logarithmic.

The last example illustrates how to plot the voltage at a node that has a name rather than a number. The first item to plot is a node voltage, the second item is the voltage across a resistor, and the third item is another node voltage, even though the second and third items both begin with the letter R. The square brackets force the interpretation of names to mean node names.

.PRINT (Print)

Purpose

The .PRINT command allows results from DC, AC, noise, and transient analyses to be an output in the form of tables, referred to as print tables in the output file.

General Form

```
.PRINT[/DGTLCHG] <analysis type> [output variable]*
```

Examples

```
.PRINT DC  V(3)  V(2,3) V(R1) I(VIN) I(R2) IB(Q13) VBE(Q13)
.PRINT AC  VM(2) VP(2) VM(3,4) VG(5) VDB(5) IR(6) II(7)
.PRINT NOISE INOISE ONOISE DB(INOISE) DB(ONOISE)
.PRINT TRAN V(3) V(2,3) ID(M2) I(VCC)
.PRINT TRAN D(QA) D(QB) V(3) V(2,3)
.PRINT/DGTLCHG TRAN QA QB RESET
.PRINT TRAN V(3) V(R1) V([RESET])
```

The last example illustrates how to print a node that has a name, rather than a number. The first item to print is a node voltage, the second item is the voltage across a resistor, and the third item to print is another node voltage, even though the second and third items both begin with the letter R. The square brackets force the names to be interpreted as node names.

Arguments and Options

[/DGTLCHG]

For digital output variables only. Values are printed for each output variable whenever one of the variables changes.

<analysis type>

Only one analysis type— DC, AC, NOISE, or TRAN—can be specified for each .PRINT command.

<output variable>

Following the analysis type is a list of the output variables. There is no limit to the number of output variables: the printout is split up depending on the width of the data columns (set using NUMDGT option) and the output width (set using WIDTH option). See **.PROBE (Probe)** for the syntax of output variables.

Comments

The values of the output variables are printed as a table where each column corresponds to one output variable. You can change the number of digits printed for analog values by using the NUMDGT option of the **.OPTIONS (Analysis Options)** command.

An analysis can have multiple .PRINT commands.

Chapter

.PROBE (Probe)

Purpose

The .PROBE command writes the results from DC, AC, and transient analyses to a data file used by Probe.

General Form

```
.PROBE[/CSDF][output variable]*
```

Examples

```
.PROBE
.PROBE V(3) V(2,3) V(R1) I(VIN) I(R2) IB(Q13) VBE(Q13)
.PROBE/CSDF
.PROBE V(3) V(R1) V([RESET])
.PROBE D(QBAR)
```

The first example (with no output variables) writes all the node voltages and all the device currents to the data file. The list of device currents written is the same as the device currents allowed as output variables.

The second example writes only those output variables specified to the data file, to restrict the size of the data file.

The third example creates a data file in a text format using the Common Simulation Data File (CSDF) format, not a binary format. This format is used for transfers between different computer families. CSDF files are larger than regular text files.

The fourth example illustrates how to specify a node that has a name rather than a number. The first item to output is a node voltage, the second item is the voltage across a resistor, and the third item to output is another node voltage, even though the second and third items both begin with the letter R. The square brackets force the interpretation of names to mean node names.

The last example writes only the output at digital node QBAR to the data file, to restrict the size of the data file.

Arguments and Options

[output variable]

This section describes the types of output variables allowed in a **.PRINT (Print)**, **.PLOT (Plot)**, and .PROBE command. Each .PRINT or .PLOT can have up to 8 output variables. This format is similar to that used when calling up waveforms while running Probe.

See the tables below for descriptions of the possible output variables. If .PROBE is used without specifying a list of output variables, all of the circuit voltages and currents are stored for post-processing. When an output variable list is included, the data stored is limited to the listed items. This form is intended for users who want to limit the size of the Probe data file.

Comments

Refer to your PSpice user's guide for a description of Probe, for information about using the Probe data file, and for more information on the use of text files in Probe. You can also consult Probe Help.

Unlike the .PRINT and .PLOT commands, there are no analysis names before the output variables. Also, the number of output variables is unlimited.

Chapter

DC Sweep and Transient Analysis Output Variables

For DC sweep and transient analysis, these are the available output variables:

General Form	Meaning of Output Variable
D(<name>)	digital value of <name> (a digital node)*
I(<name>)	current through a two terminal device
Ix(<name>)	current into a terminal of a three or four terminal device (x is one of B, D, G, or S)
Iz(<name>)	current into one end of a transmission line (z is either A or B)
V(<node>)	voltage at a node
V(<+ node>, <- node>)	voltage between two nodes
V(<name>)	voltage across a two-terminal device
Vx(<name>)	voltage at a non-grounded terminal of a device (see Ix)
Vz(<name>)	voltage at one end of a transmission line (z is either A or B)
Vxy(<name>)	voltage across two terminals of a three or four terminal device type

*These values are available for transient and DC analysis only. For the .PRINT/DGTLCHG statement, the D( ) is optional.

Example	Meaning
D(QA)	the value of digital node QA
I(D5)	current through diode D5
IG(J10)	current into gate of J10
V(3)	voltage between node three and ground
V(3,2)	voltage between nodes three and two
V(R1)	voltage across resistor R1
VA(T2)	voltage at port A of T2
VB(Q3)	voltage between base of transistor Q3 and ground
VGS(M13)	gate-source voltage of M13

Multiple-Terminal Devices

For the V(<name>) and I(<name>) forms, where <name> must be the name of a two-terminal device, the devices are:

Character ID	Two-Terminal Device
C	capacitor
D	diode
E	voltage-controlled voltage source
F	current-controlled current source
G	voltage-controlled current source
H	current-controlled voltage source)
I	independent current source
L	inductor
R	resistor
S	voltage-controlled switch
V	independent voltage source
W	current-controlled switch

For the Vx(<name>), Vxy(<name>), and Ix(<name>) forms, where <name> must be the name of a three or four-terminal device and *x* and *y* must each be a terminal abbreviation, the devices and the terminals areas follows. For the Vz(<name>) and Iz(<name>) forms, <name> must be the name of a transmission line (T device) and *z* must be A or B.

Three & Four-Terminal Device Type	Terminal Abbreviation
B (GaAs MESFET)	D (drain) G (gate) S (source)
J (Junction FET)	D (drain) G (gate) S (source)
M (MOSFET)	D (drain) G (gate) S (source) B (bulk, substrate)
Q (Bipolar transistor)	C (collector) B (base) E (emitter) S (substrate)

Three & Four-Terminal Device Type	Terminal Abbreviation
T (transmission line)	Va (near side voltage) Ia (near side current) Vb (far side voltage) Ib (far side current)
Z (IGBT)	C (collector) G (gate) E (emitter)

AC Analysis

For AC analysis, the output variables listed in the preceding section are augmented by adding a suffix.

For AC analysis, the suffixes are ignored for a .PROBE command, but can be used in a **.PRINT (Print)** command and a **.PLOT (Plot)** command, and when adding a trace in Probe. For example, in a .PROBE command, VDB(R1) is translated to V(R1), which is the raw data.

For these devices, you need to put a zero-valued voltage source in series with the device (or terminal) of interest before you can print or plot the current through this voltage source.

Suffix	Meaning of Output Variables
none	magnitude
DB	magnitude in decibels
G	group delay (-*d*PHASE/*d*FREQUENCY)
I	imaginary part
M	magnitude
P	phase in degrees
R	real part

Examples	Meaning of Output Variables for AC Analysis
II(R13)	imaginary part of current through R13
IGG(M3)	group delay of gate current for M3
IR(VIN)	real part of I through VIN
IAG(T2)	group delay of current at port A of T2
V(2,3)	magnitude of complex voltage across nodes 2 & 3
VDB(R1)	db magnitude of V across R1
VBEP(Q3)	phase of base-emitter V at Q3
VM(2)	magnitude of V at node 2

Current outputs for the F and G devices are not available for DC and transient analyses.

Noise Analysis

For noise analysis, the output variables are predefined as follows:

Output Variable	Meaning of Output Variables for Noise Analysis
INOISE	Total RMS summed noise at input node
ONOISE	INOISE equivalent at output node
DB(INOISE)	INOISE in decibels
DB(ONOISE)	ONOISE in decibels

.PRINT (Print) and **.PLOT (Plot)** cannot be used for the noise from any one device. However, the print interval on the **.NOISE (Noise Analysis)** command can be used to output this information.

.TEMP (Temperature)

Purpose The .TEMP command sets the temperature at which all analyses are done.

General Form

```
.TEMP <temperature value>*
```

Examples

```
.TEMP 125
.TEMP 0 27 125
```

Comments The temperatures are in degrees Centigrade. If more than one temperature is given, then all analyses are performed for each temperature.

It is assumed that the model parameters were measured or derived at the nominal temperature, TNOM (27°C by default). See the **.OPTIONS (Analysis Options)** command for setting TNOM.

.TEMP behaves similarly to the list variant of the **.STEP (Parametric Analysis)** statement, with the stepped variable being the temperature.

Chapter

.TF (Transfer)

Purpose

The .TF command/statement causes the small-signal DC gain to be calculated by linearizing the circuit around the bias point.

General Form

```
.TF <output variable> <input source name>
```

Examples

```
.TF V(5) VIN
.TF I(VDRIV) ICNTRL
```

Arguments and Options

<output variable>
This has the same format and meaning as in the **.PRINT (Print)** statement.

Comments

The gain from <input source name> to <output variable> and the input and output resistances are evaluated and written to the output file. This output does not require a .PRINT (Print), **.PLOT (Plot)**, or **.PROBE (Probe)** statement.When <output variable> is a current, it is restricted to be the current through a voltage source.

The results of the .TF command are only available in the output file. They cannot be viewed in Probe.

Chapter

.TRAN (Transient Analysis)

Purpose

The .TRAN command causes a transient analysis to be performed on the circuit and specifies the time period for the analysis.

General Form

```
.TRAN[/OP] <print step value> <final time value>
+[no-print value [step ceiling value]][SKIPBP]
```

Examples

```
.TRAN 1ns 100ns
.TRAN/OP 1ns 100ns 20ns SKIPBP
.TRAN 1ns 100ns 0ns .1ns
```

Arguments and Options

[/OP]

Causes the same detailed printing of the bias point that the **.OP (Bias Point)** command does for the regular bias point. Without using this option, only the node voltages are printed for the transient analysis bias point.

<print step value>

Sets the time interval used for printing (.PRINT), plotting (.PLOT), or performing a Fourier integral on (.FOUR) the results of the transient analysis.

Since the results are computed at different times than they are printed, a 2nd-order polynomial interpolation is used to obtain the printed values. This applies only to **.PRINT (Print)**, **.PLOT (Plot)**, and **.FOUR (Fourier Analysis)** outputs and does not affect Probe.

<final time value>

Sets the end time for the analysis.

[no-print value]

Sets the time interval (from TIME=0) that is not printed, plotted, or given to Probe.

[step ceiling value]

Overrides the default ceiling on the internal time step with a lower value.

[SKIPBP]

Skips calculation of the bias point.

When this option is used, the bias conditions are fully determined by the IC= specifications for capacitors and inductors.

Chapter

Comments

The transient analysis calculates the circuit's behavior over time, always starting at TIME=0 and finishing at <final time value>, but you can suppress the output of a portion of the analysis. Use a **.PRINT (Print)**, **.PLOT (Plot)**, **.FOUR (Fourier Analysis)**, or **.PROBE (Probe)** to get the results of the transient analysis.

Prior to performing the transient analysis, PSpice computes a bias point for the circuit separate from the regular bias point. This is necessary because at the start of a transient analysis, the independent sources can have different values than their DC values.

The internal time step of the transient analysis adjusts as the analysis proceeds: over intervals when there is little activity, the time step is increased, and during busy intervals it is decreased. The default ceiling on the internal time step is <final time value>/50, but when there are no charge storage elements, inductances, or capacitances in the circuit, the ceiling is <print step value>.

The .TRAN command also sets the variables TSTEP and TSTOP, which are used in defaulting some waveform parameters. TSTEP is equal to <print step value> and TSTOP is equal to <final time value>.

Refer to your PSpice user's guide for more information on setting initial conditions.

* (Comment)

Purpose

A statement beginning with an asterisk * is a comment line, which PSpice ignores.

General Form

```
* [any text]
```

Examples

```
* This is an example of
* a multiple-line comment
```

Comments

Use an asterisk at the beginning of each line you want to be a comment. A single asterisk does not extend to subsequent lines. For example:

```
* .MODEL ABC NMOS (. . . .
+ . . . .)
```

produces an error message, because the second line is not covered by the first asterisk.

The use of comment statements throughout the input is recommended. It is good practice to insert a comment line just before a subcircuit definition to identify the nodes, for example:

```
*                +IN  -IN  V+  V-  +OUT  -OUT
.SUBCKT  OPAMP  100  101  1   2    200   201
```

or to identify major blocks of circuitry.

; (In-line Comment)

Purpose

A semicolon ; is treated as the end of a line.

General Form

```
circuit file text ;[any text]
```

Examples

```
R13 6 8 10  ; R13 is a
            ; feedback resistor
C3 15 0 .1U ; decouple supply
```

Comments

The simulator moves on to the next line in the circuit file. The text on the line after the semicolon ; is a comment and has no effect. The use of comments throughout the input is recommended. This type of comment can also replace comment lines, which must start with * in the first column.

Trailing in-line comments that extend to more that one line can use a semicolon to mark the beginning of the subsequent comment lines, as shown in the example.

Chapter

+ (Line Continuation)

Purpose A plus sign + is treated as the continuation of the previous line.

General Form

```
circuit file text
+ more text
```

Examples

```
.DISTRIBUTION bi_modal (-1,1) (-.5,1) (-.5,0) (.5,0)
+ (.5,1) (1,1)
```

Comments Because the simulator reads the line preceded by a plus sign as a continuation of the previous line, you can use the plus sign to break up long lines of command text.

Analog Devices

Letter	Device Type	Letter	Device Type
B	GaAsFET	N	Digital Input (N Device)
C	Capacitor	O	Digital Output (O Device)
D	Diode	Q	Bipolar Transistor
E	Voltage-Controlled Voltage Source	R	Resistor
F	Current-Controlled Current Source	S	Voltage-Controlled Switch
G	Voltage-Controlled Current Source	T	Transmission Line
H	Current-Controlled Voltage Source	U	Digital Primitive Summary
I	Independent Current Source & Stimulus	U STIM	Stimulus Devices
J	Junction FET	V	Independent Voltage Source & Stimulus
K	Inductor Coupling (and Magnetic Core)	W	Current-Controlled Switch
K	Transmission Line Coupling	X	Subcircuit Instantiation
L	Inductor	Z	IGBT
M	New! MOSFET		

Digital Devices

Commands

Index

Glossary

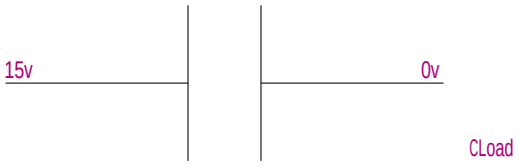
Capacitor

General Form `C<name> <(+) node> <(-) node> [model name] <value> [IC=<initial value>]`

Examples

```
CLOAD 15 0 20pF
C2 1 2 .2E-12 IC=1.5V
CFDBCK  3 33 CMOD 10pF
```

Model Form `.MODEL  <model name> CAP [model parameters]`



Arguments and Options

(+) and (-) nodes

Define the polarity when the capacitor has a positive voltage across it. The first node listed (or pin one in Schematics) is defined as positive. The voltage across the component is therefore defined as the first node voltage less the second node voltage.

[model name]

If [model name] is left out, then <value> is the capacitance in farads. If [model name] is specified, then the value is given by the model parameters; see **Capacitor Value Formula**.

<initial value>

The initial voltage across the capacitor during the bias point calculation. It can also be specified in a circuit file using a .IC command as follows:

```
.IC V(+node, -node) <initial value>
```

Comments

Positive current flows from the (+) node through the capacitor to the (-) node. Current flow from the first node through the component to the second node is considered positive.

For details on using the .IC command in a circuit file, see **.IC (Initial Bias Point Condition)** and refer to your PSpice user's guide for more information.

The initial voltage across the capacitor can also be set in Schematics by using the IC1 symbol if the capacitor is connected to ground or by using the IC2 symbol for setting the initial conditions between two nodes. These symbols can be found in `special.slb`.

For more information about setting initial conditions, refer to the Schematics User's Guide if you are using Schematics, or refer to your PSpice user's guide if you are using PSpice.

Chapter

Schematics Symbols

For standard C parts, the effective value of the part is set directly by the VALUE attribute. For the variable capacitor, C_VAR, the effective value is the product of the base value (VALUE) and multiplier (SET).

In general, capacitors should have positive component values (VALUE attribute). In all cases, components must not be given a value of zero.

However, there are cases when negative component values are desired. This occurs most often in filter designs that analyze an RLC circuit equivalent to a real circuit. When transforming from the real to the RLC equivalent, it is possible to end up with negative component values.

PSpice A/D allows negative component values for bias point, DC sweep, AC, and noise analyses. A transient analysis may fail for a circuit with negative components. Negative capacitors may create instabilities in time that the analysis cannot handle.

Symbol Name	Model Type	Attribute	Attribute Description
C	capacitor	VALUE	capacitance
		IC	initial voltage across the capacitor during bias point calculation
C_VAR		VALUE	base capacitance
		SET	multiplier

Breakout Parts

For non-stock passive and semiconductor devices, Schematics provides a set of breakout parts designed for customizing model parameters for simulation. These are useful for setting up Monte Carlo and worst-case analyses with device and/or lot tolerances specified for individual model parameters. Another approach is to use the model editor to derive an instance model and customize this. For example, you could add device and/or lot tolerances to model parameters.

Basic breakout part names consist of the intrinsic PSpice A/D device letter plus the suffix BREAK. By default, the model name is the same as the part name and references the appropriate device model with all parameters set at their default. For instance, the DBREAK part references the DBREAK model which is derived from the intrinsic PSpice A/D D model (.MODEL DBREAK D).

For breakout part CBREAK, the effective value is computed from a formula that is a function of the specified VALUE attribute.

Part Type	Symbol Name	Symbol Library	Attribute	Description
capacitor	CBREAK	`breakout.slb`	VALUE	capacitance
			IC	initial voltage across the capacitor during bias point calculation
			MODEL	CAP model name

Capacitor Model Parameters

Model Parameters*	Description	Units	Default
C	capacitance multiplier		1.0
TC1	linear temperature coefficient	$°C^{-1}$	0.0
TC2	quadratic temperature coefficient	$°C^{-2}$	0.0
T_ABS	absolute temperature	°C	
T_MEASURED	measured temperature	°C	
T_REL_GLOBAL	relative to current temperature	°C	
T_REL_LOCAL	relative to AKO model temperature	°C	
VC1	linear voltage coefficient	$volt^{-1}$	0.0
VC2	quadratic voltage coefficient	$volt^{-2}$	0.0

* For information on **T_MEASURED**, **T_ABS**, **T_REL_GLOBAL**, and **T_REL_LOCAL**, see **.MODEL (Model)**.

Capacitor Equations

Capacitor Value Formula

If [model name] is specified, then the value is given by:

$$\langle value\rangle \cdot C \cdot (1+\mathbf{VC1}\cdot V+\mathbf{VC2}\cdot V^2)\cdot(1+\mathbf{TC1}\cdot(T-Tnom)+\mathbf{TC2}\cdot(T-Tnom)^2)$$

where <value> is normally positive (though it can be negative, but not zero). Tnom is the nominal temperature (set using TNOM option).

Capacitor Equation for Noise

The capacitor does not have a noise model.

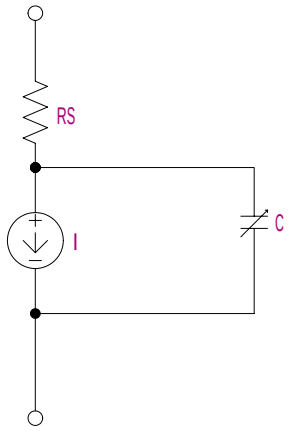
Diode

General Form `D<name> <(+) node> <(-) node> <model name> [area value]`

Examples
```
DCLAMP 14  0 DMOD
D13 15 17 SWITCH 1.5
```

Model Form `.MODEL <model name> D [model parameters]`

Description The diode is modeled as an ohmic resistance (**RS**/area) in series with an intrinsic diode. Positive current is current flowing from the anode through the diode to the cathode.



Arguments and Options

<(+) node>
The anode.

<(-) node>
The cathode.

[area value]
Scales **IS**, **ISR**, **IKF**,**RS**, **CJO**, and **IBV**, and has a default value of 1. **IBV** and **BV** are both specified as positive values.

Chapter

Schematics Symbols

The following table lists the set of diode breakout parts designed for customizing model parameters for simulation. These are useful for setting up Monte Carlo and worst-case analyses with device and/or lot tolerances specified for individual model parameters.

Symbol Name	Model Type	Attribute	Attribute Description
DBREAK DBREAK3 DBREAKCR DBREAKVV DBREAKZ	D, X	MODEL	D model name

Setting operating temperature

Operating temperature can be set to be different from the global circuit temperature by defining one of the model parameters: T_ABS, T_REL_GLOBAL, or T_REL_LOCAL. Additionally, model parameters can be assigned unique measurement temperatures using the T_MEASURED model parameter. For more information, see **Special Considerations**.

Diode Model Parameters

Model Parameters*	Description	Unit	Default
AF	flicker noise exponent		1.0
BV	reverse breakdown knee voltage	volt	infinite
CJO	zero-bias p-n capacitance	farad	0.0
EG	bandgap voltage (barrier height)	eV	1.11
FC	forward-bias depletion capacitance coefficient		0.5
IBVL	low-level reverse breakdown knee current	amp	0.0
IBV	reverse breakdown knee current	amp	1E-10
IKF	high-injection knee current	amp	infinite
IS	saturation current	amp	1E-14
ISR	recombination current parameter	amp	0.0
KF	flicker noise coefficient		0.0
M	p-n grading coefficient		0.5
N	emission coefficient		1.0
NBV	reverse breakdown ideality factor		1.0
NBVL	low-level reverse breakdown ideality factor		1.0
NR	emission coefficient for isr		2.0
RS	parasitic resistance	ohm	0.0
TBV1	bv temperature coefficient (linear)	$°C^{-1}$	0.0
TBV2	bv temperature coefficient (quadratic)	$°C^{-2}$	0.0
TIKF	ikf temperature coefficient (linear)	$°C^{-1}$	0.0
TRS1	rs temperature coefficient (linear)	$°C^{-1}$	0.0
TRS2	rs temperature coefficient (quadratic)	$°C^{-2}$	0.0
TT	transit time	sec	0.0
T_ABS	absolute temperature	°C	
T_MEASURED	measured temperature	°C	
T_REL_GLOBAL	relative to current temperature	°C	
T_REL_LOCAL	Relative to AKO model temperature	°C	
VJ	*p-n* potential	volt	1.0
XTI	IS temperature exponent		3.0

* For more information on **T_MEASURED**, **T_ABS**, **T_REL_GLOBAL**, and **T_REL_LOCAL**, see **.MODEL (Model)**.

Diode Equations

The equations in this section use the following variables:

Vd	= voltage across the intrinsic diode only
Vt	= $k \cdot T/q$ (thermal voltage)
k	= Boltzmann's constant
q	= electron charge
T	= analysis temperature (°K)
Tnom	= nominal temperature (set using TNOM option)

Other variables are listed in **Diode Model Parameters**.

Diode Equations for DC Current

Id = *area*·(Ifwd - Irev)

Ifwd = forward current = Inrm·Kinj + Irec·Kgen

Inrm = normal current = IS·($e^{Vd/(N \cdot Vt)}$-1)

if: **IKF** > 0
then: Kinj = high-injection factor = (**IKF**/(**IKF**+Inrm))$^{1/2}$
else: Kinj = 1

Irec = recombination current = **ISR**·($e^{Vd/(NR \cdot Vt)}$-1)

Kgen = generation factor = ((1-Vd/VJ)^2+0.005)$^{M/2}$

Irev = reverse current = $Irev_{high}$ + $Irev_{low}$

$Irev_{high}$ = **IBV**·$e^{-(Vd+BV)/(NBV \cdot Vt)}$

$Irev_{low}$ = **IBVL**·$e^{-(Vd+BV)/(NBVL \cdot Vt)}$

Diode Equations for Capacitance

Cd = Ct + *area*·Cj

Ct = transit time capacitance = **TT**·Gd

Gd = DC conductance = area · $\frac{d(Inrm \cdot Kinj + Irec \cdot Kgen)}{dVd}$

Kinj = high-injection factor

Cj = **CJO**·(1-Vd/VJ)^M IF: Vd ≤ **FC**·**VJ**

Cj = **CJO**·(1-**FC**)$^{-(1+M)}$·(1-**FC**·(1+**M**)+**M**·Vd/**VJ**) IF: Vd > FC·VJ

Cj = junction capacitance

Diode Equations for Temperature Effects

IS(T) = **IS**·$e^{(T/Tnom-1)\cdot EG/(N\cdot Vt)}$·$(T/Tnom)^{XTI/N}$

ISR(T) = **ISR**·$e^{(T/Tnom-1)\cdot EG/(NR\cdot Vt)}$·$(T/Tnom)^{XTI/NR}$

IKF(T) = **IKF**·(1 + **TIKF**·(T-Tnom))

BV(T) = **BV**·(1 + **TBV1**·(T-Tnom) + **TBV2**·$(T-Tnom)^2$)

RS(T) = **RS**·(1 + **TRS1**·(T-Tnom) + **TRS2**·$(T-Tnom)^2$)

VJ(T) = **VJ**·T/Tnom - 3·Vt·*ln*(T/Tnom) - Eg(Tnom)·T/Tnom + Eg(T)

Eg(T) = silicon bandgap energy = 1.16 - .000702·T^2/(T+1108)

CJO(T) = **CJO**·(1 + **M**·(.0004·(T-Tnom)+(1-**VJ**(T)/**VJ**)))

Diode Equations for Noise

Noise is calculated assuming a 1.0-hertz bandwidth, using the following spectral power densities (per unit bandwidth).

Parasitic Resistance Thermal Noise

$In^2 = 4 \cdot k \cdot T/(\mathbf{RS}/area)$

Intrinsic Diode Shot and Flicker Noise

$In^2 = 2 \cdot q \cdot Id + \mathbf{KF} \cdot Id^{AF}/FREQUENCY$

References

For a detailed description of p-n junction physics, refer to:

[1] A. S. Grove, Physics and Technology of Semiconductor Devices, John Wiley and Sons, Inc., 1967.

Also, for a generally detailed discussion of the U.C. Berkeley SPICE models, including the diode device, refer to:

[2] P. Antognetti and G. Massobrio, Semiconductor Device Modeling with SPICE, McGraw-Hill, 1988.

Section

Voltage-Controlled Voltage Source

Voltage-Controlled Current Source

General Form

```
E<name> <(+) node> <(-) node> <(+) controlling node> <(-) controlling
node> <gain>

E<name> <(+) node> <(-) node> POLY(<value>)
+ < <(+) controlling node> <(-) controlling node> >*
+ < <polynomial coefficient value> >*

E<name> <(+) <node> <(-) node> VALUE = { <expression> }

E<name> <(+) <node> <(-) node> TABLE { <expression> } =
+ < <input value>,<output value> >*

E<name> <(+) node> <(-) node> LAPLACE { <expression> } =
+ { <transform> }

E<name> <(+) node> <(-) node> FREQ { <expression> } = [KEYWORD]
+ < <frequency value>,<magnitude value>,<phase value> >*
+ [DELAY = <delay value>]

E<name> <(+) node> <(-) node> CHEBYSHEV { <expression> } =
+ <[LP] [HP] [BP] [BR]>,<cutoff frequencies>*,<attenuation>*
```

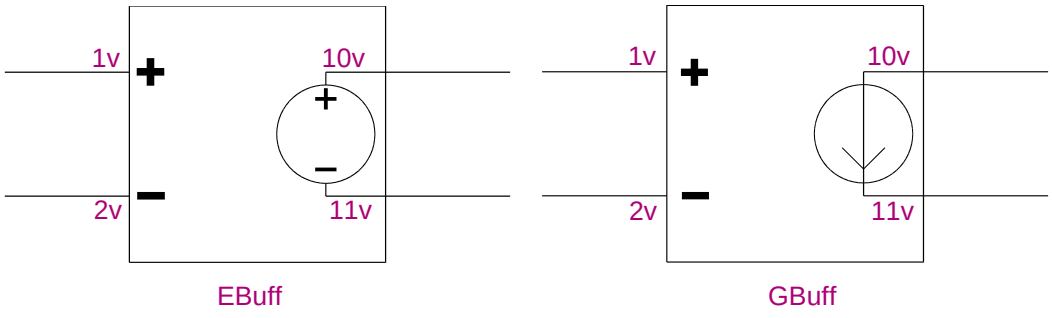
Examples

```
EBUFF 1 2 10 11 1.0
EAMP 13 0 POLY(1) 26  0 0 500
ENONLIN 100 101 POLY(2) 3 0  4 0  0.0 13.6 0.2 0.005
ESQROOT   5   0 VALUE = {5V*SQRT(V(3,2))}
ET2 2 0 TABLE {V(ANODE,CATHODE)} = (0,0) (30,1)
ERC 5 0 LAPLACE {V(10)} = {1/(1+.001*s)}
ELOWPASS 5 0 FREQ {V(10)}=(0,0,0)(5kHz, 0,0)(6kHz -60, 0) DELAY=3.2ms
ELOWPASS 5 0 CHEBYSHEV {V(10)} = LP 800 1.2K .1dB 50dB

GBUFF 1 2 10 11  1.0
GAMP 13 0 POLY(1) 26  0 0 500
GNONLIN 100 101 POLY(2) 3 0 4 0 0.0 13.6 0.2 0.005
GPSK 11 6 VALUE = {5MA*SIN(6.28*10kHz*TIME+V(3))}
GT ANODE CATHODE VALUE = {200E-6*PWR(V(1)*V(2),1.5)}
GLOSSY 5 0 LAPLACE {V(10)} = {exp(-sqrt(C*s*(R+L*s)))}
```

Description

The Voltage-Controlled Voltage Source (E) and the Voltage-Controlled Current Source (G) devices have the same syntax. For a Voltage-Controlled Current Source just substitute G for E. G generates a current, whereas E generates a voltage.



Chapter

Arguments and Options

POLY(<value>)
Specifies the number of dimensions of the polynomial. The number of pairs of controlling nodes must be equal to the number of dimensions.

(+) and (-) nodes
Output nodes. Positive current flows from the (+) node through the source to the (-) node.

The <(+) controlling node> and <(-) controlling node>
Are in pairs and define a set of controlling voltages. A particular node can appear more than once, and the output and controlling nodes need not be different. The TABLE form has a maximum size of 2048 input/output value pairs.

FREQ
If a DELAY value is specified, the simulator modifies the phases in the FREQ table to incorporate the specified delay value. This is useful for cases of tables which the simulator identifies as being non-causal. When this occurs, the simulator provides a delay value necessary to make the table causal. The new syntax allows this value to be specified in subsequent simulation runs, without requiring the user to modify the table.

If a KEYWORD is specified for FREQ tables, it alters the values in the table. The KEYWORD can be one of the following:

- MAG causes magnitude of frequency response to be interpreted as a raw value instead of dB.
- DB causes magnitude to be interpreted as dB (the default).
- RAD causes phase to be interpreted in radians.
- DEG causes phase to be interpreted in degrees (the default).
- R_I causes magnitude and phase values to be interpreted as real and imaginary magnitudes.

Comments

The first form and the first two examples apply to the linear case; the second form and the third example are for the nonlinear case. The last five forms and examples are analog behavioral modeling (ABM) that have expression, look up table, Laplace transform, frequency response, and filtering. Refer to your PSpice user's guide for more information on analog behavioral modeling.

Chebyshev filters have two attenuation values, given in dB, which specify the pass band ripple and the stop band attenuation. They can be given in either order, but must appear after all of the cutoff frequencies have been given. Low pass (LP) and high pass (HP) have two cutoff frequencies, specifying the pass band and stop band edges, while band pass (BP) and band reject (BR) filters have four. Again, these can be given in any order.

A listing of the filter Laplace coefficients can be obtained for each stage by turning on the LIST option in Schematics (in the Analysis Setup dialog box, click Options). The output is written to the .out file after the simulation is complete.

For the linear case, there are two controlling nodes and these are followed by the gain. For all cases, including the nonlinear case (POLY), refer to your PSpice user's guide.

Expressions **cannot** be used for linear and polynomial coefficient values in a voltage-controlled voltage source device statement.

Basic SPICE Polynomial Expressions (POLY)

PSpice A/D (and SPICE) use the following syntax:

```
<controlled source> <connecting nodes>
+POLY(<dimension>) <controlling input> <coefficients>
```

where

<controlled source>	is <[E][F][G][H]device name>, meaning the device type is one of E, F, G, or H
<connecting nodes>	specifies <(+node_name, -node_name)> pair between which the device is connected
<dimension>	is the dimension <value> of the polynomial describing the controlling function
<controlling input>	specifies <(+node_name, -node_name)>* pairs used as input to the voltage controlled source (device types E and G), or <V device name>* for the current controlled source (device types F and H), and where the number of controlling inputs for either case equals <dimension>
<coefficients>	specifies the coefficient <values>* for the polynomial transfer function

If the source is one-dimensional (there is only one controlling source), POLY(1) is required unless the linear form is used. If the source is multidimensional (there is more than one controlling source), the dimension needs to be included in the keyword, for instance POLY(2).

Caution must be exercised with the POLY form. For instance,

```
EWRONG 1 0 POLY(1) (1,0) .5 1.0
```

tries to set node 1 to .5 volts greater than node 1. In this case, any analyses which you specify will fail to calculate a result. In particular, PSpice A/D cannot calculate the bias point for a circuit containing EWRONG. This also applies to the VALUE form of EWRONG:

```
(EWRONG 1 0 VALUE = {0.5 * V(1)}).
```

Basic Controlled Source Attributes

Symbol Name	Attribute	Description
E	GAIN	gain
F		gain
G		transconductance
H		transresistance
EPOLY, FPOLY, GPOLY, HPOLY	COEFF	polynomial coefficient

PSpice A/D has a built-in capability allowing controlled sources to be defined with a polynomial transfer function of any degree and any dimension. Polynomials have associated

coefficients for each term. Consider a voltage-controlled source with voltages V_1, V_2, ... V_n. The coefficients are associated with the polynomial according to this convention:

$$\begin{aligned}
&Vout = P_0 + \\
&P_1 \cdot V_1 + P_2 \cdot V_2 + \cdots P_n \cdot V_n + \\
&P_{n+1} \cdot V_1 \cdot V_1 + P_{n+2} \cdot V_1 \cdot V_2 + \cdots P_{n+n} \cdot V_1 \cdot V_n + \\
&P_{2n+1} \cdot V_2 \cdot V_2 + P_{2n+2} \cdot V_2 \cdot V_3 + \cdots P_{2n+n-1} \cdot V_2 \cdot V_n + \\
&\quad\vdots \\
&P_{n!/(2(n-2)!)+2n} \cdot V_n \cdot V_n + \\
&P_{n!/(2(n-2)!)+2n+1} \cdot V_1^2 \cdot V_1 + P_{n!/(2(n-2)!)+2n+2} \cdot V_1^2 \cdot V_2 + \cdots \\
&\quad\vdots
\end{aligned}$$

The above is written for a voltage-controlled voltage source, but the form is similar for the other sources.

The POLY part types shown in **Basic Controlled Source Attributes** are defined with a dimension of one, meaning there is only one controlling source. However, similar parts can be defined of any degree and dimension by creating part symbols with appropriate coefficient and TEMPLATE attributes, and the appropriate number of input pins.

The current-controlled parts (F, FPOLY, H, and HPOLY), contain a current-sensing voltage source. When netlisted, they generate two device declarations to the circuit file set: one for the controlled source and one for the independent current-sensing voltage source.

When defining a current-controlled source symbol of higher dimension, the TEMPLATE attribute must account for the same number of current-sensing voltage sources (equal to the dimension value). For example, a two dimensional current-controlled voltage source is described by the following polynomial equation:

$$Vout = C_0 + C_1 I_1 + C_2 I_2 + C_{11} I_1^2 + C_{12} I_1 I_2 + C_{22} I_2^2$$

To create the two dimensional HPOLY2 symbol, these attributes must be defined:

```
COEFF0 = 1
COEFF1 = 1
COEFF2 = 1
COEFF11 = 1
COEFF12 = 1
COEFF22 = 1
COEFFS = @COEFF0 @COEFF1 @COEFF2 @COEFF11 @COEFF12 @COEFF22
TEMPLATE = H^@REFDES %5 %6 POLY(2) VH1^@REFDES VH2^@REFDES
\n+ @COEFFS \nVH1^@REFDES %1 %2 0V \nVH2^@REFDES %3 %4 0V
```

The TEMPLATE definition is actually contained on a single line. The VH1 and VH2 fragments after the \n characters represent the device declarations for the two current-sensing voltage sources required by this part. Also, the symbol graphics must have the appropriate number of pins. When placing an instance of HPOLY2 in your schematic, the COEFF*n* attributes must be appropriately set.

Implementation Examples

Following are some examples of traditional SPICE POLY constructs and equivalent ABM parts which could be used instead.

Example 1: Four-Input Voltage Adder

This is an example of a device which takes four input voltages and sums them to provide a single output voltage.

The representative polynomial expression would be as follows:

$V_{out} = 0.0 + (1.0)V_1 + (1.0)V_2 + (1.0)V_3 + (1.0)V_4$

The corresponding SPICE POLY form would be as follows:

```
ESUM 100 101 POLY(4) (1,0) (2,0) (3,0) (4,0) 0.0 1.0 1.0
+  1.0 1.0
```

This could be represented with a single ABM expression device configured with the following expression attributes:

```
EXP1 = V(1,0) +
EXP2 = V(2,0) +
EXP3 = V(3,0) +
EXP4 = V(4,0)
```

Following template substitution for the ABM device, the output becomes:

```
V(OUT) = { V(1,0) + V(2,0) + V(3,0) + V(4,0) }
```

Example 2: Two-Input Voltage Multiplier

This is an example of a device which takes two input voltages and multiplies them together resulting in a single output voltage.

The representative polynomial expression would be as follows:

$V_{out} = 0.0 + (0.0)V_1 + (0.0)V_2 + (0.0)V_1^2 + (1.0)V_1V_2$

The corresponding SPICE POLY form would be as follows:

```
EMULT 100 101 POLY(2) (1,0) (2,0) 0.0 0.0 0.0 0.0 1.0
```

This could be represented with a single MULT device. For additional examples of a voltage multiplier device, refer to the Analog Behavioral Modeling chapter of your PSpice user's guide.

Example 3: Voltage Squarer

This is an example of a device that outputs the square of the input value.

For the one-dimensional polynomial, the representative polynomial expression reduces to:

$Vout = P_0 + P_1 \cdot V + P_2 \cdot V^2 + \ldots P_n \cdot V^n$

The corresponding SPICE POLY form would be as follows:

```
ESQUARE 100 101 POLY(1) (1,0) 0.0 0.0 1.0
```

This could be represented by a single instance of the MULT part, with both inputs from the same net. This results in the following:

$V_{out} = (V_{in})^2$

Section

Current-Controlled Current Source

Current-Controlled Voltage Source

General Form

```
F<name> <(+) node> <(-) node>
+ <controlling V device name> <gain>

F<name> <(+) node> <(-) node> POLY(<value>)
+ <controlling V device name>*
+ < <polynomial coefficient value> >*
```

Examples

```
FSENSE 1 2 VSENSE 10.0
FAMP 13 0 POLY(1) VIN 0 500
FNONLIN 100 101 POLY(2) VCNTRL1 VCINTRL2 0.0 13.6 0.2 0.005
```

Description

The Current-Controlled Current Source (F) and the Current-Controlled Voltage Source (H) devices have the same syntax. For a Current-Controlled Voltage Source just substitute an H for the F. The H device generates a voltage, whereas the F device generates a current.

Arguments and Options

(+) and (-)

Output nodes. A positive current flows from the (+) node through the source to the (-) node. The current through the controlling voltage source determines the output current. The controlling source must be an independent voltage source (V device), although it need not have a zero DC value.

POLY(<value>)

Specifies the number of dimensions of the polynomial. The number of controlling voltage sources must be equal to the number of dimensions.

Comments

The first General Form and the first two examples apply to the linear case. The second form and the last example are for the nonlinear case.

For the linear case, there must be one controlling voltage source and its name is followed by the gain. For all cases, including the nonlinear case (POLY), refer to your PSpice user's guide.

Expressions cannot be used for linear and polynomial coefficient values in a current-controlled current source device statement.

Basic SPICE Polynomial Expressions (POLY)

For more information on the POLY form, see **Basic SPICE Polynomial Expressions (POLY)**.

Chapter

Independent Current Source & Stimulus

Independent Voltage Source & Stimulus

General Form

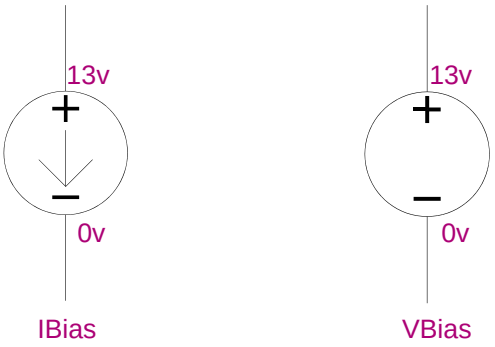
```
I<name> <(+) node> <(-) node>
+ [ [DC] <value> ]
+ [ AC <magnitude value> [phase value] ]
+ [STIMULUS=<stimulus name>]
+ [transient specification]
```

Examples

```
IBIAS 13 0 2.3mA
IAC 2 3 AC .001
IACPHS 2 3 AC .001 90
IPULSE 1 0 PULSE(-1mA 1mA 2ns 2ns 2ns 50ns 100ns)
I3 26 77 DC .002 AC 1 SIN(.002 .002 1.5MEG)
```

Description

This element is a current source. Positive current flows from the (+) node through the source to the (-) node: in the first example, IBIAS drives node 13 to have a negative voltage. The default value is zero for the DC, AC, and transient values. None, any, or all of the DC, AC, and transient values can be specified. The AC phase value is in degrees. The pulse and exponential examples are explained later in this section.



The Independent Current Source & Stimulus (I) and the Independent Voltage Source & Stimulus (V) devices have the same syntax. For an Independent Voltage Source & Stimulus just substitute a V for the I. The V device functions identically and has the same syntax as the I device, except that it generates voltage instead of current.

The variables TSTEP and TSTOP, which are used in defaulting some waveform parameters, are set by the **.TRAN (Transient Analysis)** command. TSTEP is <print step value> and TSTOP is <final time value>. The .TRAN command can be anywhere in the circuit file; it need not come after the voltage source.

Chapter

Arguments and Options

<stimulus name>
References a **.STIMULUS (Stimulus)** definition.

[transient specification]

Use this value...	To produce this result...
EXP (<parameters>)	an exponential waveform
PULSE (<parameters>)	a pulse waveform
PWL (<parameters>)	a piecewise linear waveform
SFFM (<parameters>)	a frequency-modulated waveform
SIN (<parameters>)	a sinusoidal waveform

Independent Current Source & Stimulus (EXP)

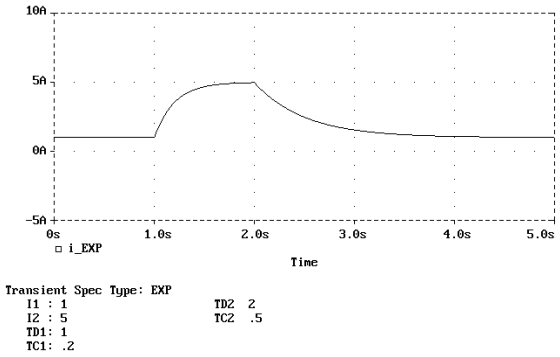
General Form `EXP (<i1> <i2> <td1> <tc1> <td2> <tc2>)`

Examples `IRAMP 10 5 EXP(1 5 1 .2 2 .5)`

Waveform Parameters

Parameter	Description	Units	Default
<i1>	Initial current	amp	none
<i2>	Peak current	amp	none
<td1>	Rise (fall) delay	sec	0
<tc1>	Rise (fall) time constant	sec	**TSTEP**
<td2>	Fall (rise) delay	sec	<td1>+**TSTEP**
<tc2>	Fall (rise) time constant	sec	**TSTEP**

Description The EXP form causes the current to be <i1> for the first <td1> seconds. Then, the current decays exponentially from <i1> to <i2> using a time constant of <tc1>. The decay lasts td2-td1 seconds. Then, the current decays from <i2> back to <i1> using a time constant of <tc2>. **Independent Current Source and Stimulus Exponential Waveform Formulas** describe the EXP waveform.



Independent Current Source and Stimulus Exponential Waveform Formulas

Time Period	Value
0 to <td1>	i1
<td1> to <td2>	$i1 + (i2-i1)\cdot(1-e^{-(TIME-td1)/tc1})$
<td2> to TSTOP	$i1 + (i2-i1)\cdot((1-e^{-(TIME-td1)/tc1})-(1-e^{-(TIME-td2)/tc2}))$

Independent Current Source & Stimulus (PULSE)

General Form `PULSE (<i1> <i2> <td> <tr> <tf> <pw> <per>)`

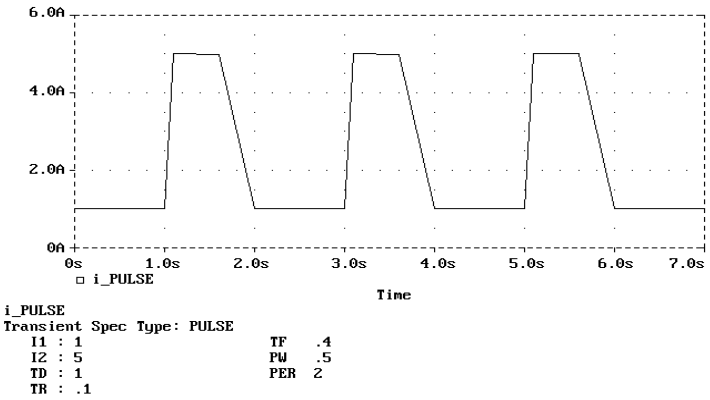
Example `ISW 10 5 PULSE(1A 5A 1sec .1sec .4sec .5sec 2sec)`

Waveform Parameters

Parameters	Description	Units	Default
<i1>	Initial current	amp	none
<i2>	Pulsed current	amp	none
<td>	Delay	sec	0
<tf>	Fall time	sec	**TSTEP**
<tr>	Rise time	sec	**TSTEP**
<pw>	Pulse width	sec	**TSTOP**
<per>	Period	sec	**TSTOP**

Description

The PULSE form causes the current to start at <i1>, and stay there for <td> seconds. Then, the current goes linearly from <i1> to <i2> during the next <tr> seconds, and then the current stays at <i2> for <pw> seconds. Then, it goes linearly from <i2> back to <i1> during the next <tf> seconds. It stays at <i1> for per-(tr+pw+tf) seconds, and then the cycle is repeated except for the initial delay of <td> seconds. **Independent Current Source and Stimulus Pulse Waveform Formulas** describe the PULSE waveform.



Independent Current Source and Stimulus Pulse Waveform Formulas

Time	Value
0	i1
td	i1
td+tr	i2
td+tr+pw	i2
td+tr+pw+tf	i1
td+per	i1
td+per+tr	i2
.	.
.	.
.	.

Independent Current Source & Stimulus (PWL)

General Form

```
PWL
+ [TIME_SCALE_FACTOR=<value>]
+ [VALUE_SCALE_FACTOR=<value>]
+ (corner_points)*
```

where `corner_points` are:

`(<tn>, <in>)`	to specify a point
`FILE <filename>`	to read point values from a file
`REPEAT FOR <n> (corner_points)*`	
`ENDREPEAT`	to repeat <n> times
`REPEAT FOREVER (corner_points)*`	
`ENDREPEAT`	to repeat forever

Examples

```
v1     1 2    PWL    (0,1) (1.2,5) (1.4,2) (2,4) (3,1)
```

```
v2             3 4    PWL    REPEAT FOR 5 (1,0) (2,1) (3,0) ENDREPEAT
v3             5,6    PWL    REPEAT FOR 5 FILE DATA1.TAB
+                            ENDREPEAT
v4             7 8    PWL    TIME_SCALE_FACTOR=0.1
+                     REPEAT FOREVER
+                            REPEAT FOR 5 (1,0) (2,1) (3,0) ENDREPEAT
+                            REPEAT FOR 5 FILE DATA1.TAB
+                            ENDREPEAT
+                     ENDREPEAT
```

n volt square wave (where n is 1, 2, 3, 4, then 5); 75% duty cycle; 10 cycles; 1 microseconds per cycle:

```
.PARAM  N=1
.STEP PARAM  N    1,5,1
V1  1  0  PWL
+      TIME_SCALE_FACTOR=1e-6 ;all time units are scaled to
+      microseconds
+      REPEAT FOR 10
+      (.25, 0)(.26, {N})(.99, {N})(1, 0)
+      ENDREPEAT
```

5 volt square wave; 75% duty cycle; 10 cycles; 10 microseconds per cycle; followed by 50% duty cycle n volt square wave (where n is 1, 2, 3, 4, then 5) lasting until the end of simulation:

```
.PARAM  N=.2
.STEP PARAM  N    .2,  1.0,  .2
V1  1  0  PWL
+             TIME_SCALE_FACTOR=1e-5  ; all time units are
+             scaled to 10 us
+             VALUE_SCALE_FACTOR=5
+             REPEAT FOR 10
+             (.25, 0)(.26, 1)(.99, 1)(1, 0)
+             ENDREPEAT


+             REPEAT FOREVER
+             (+.50, 0)
+             (+.01, {N})   ; iteration time .51
+             (+.48, {N})   ; iteration time .99
+             (1, 0)
+             ENDREPEAT
```

Assuming that a PWL specification has been given for a device to generate two triangular waveforms:

```
V3     1 0  PWL (1ms, 1)(2ms, 0)(3ms, 1)(4ms, 0)
```

Or, to replace the above with

```
V3  1  0  PWL  FILE  TRIANGLE.IN
```

where the file `triangle.in` would need to contain:

```
(1ms, 1)(2ms, 0)(3ms, 1)(4ms, 0)
```

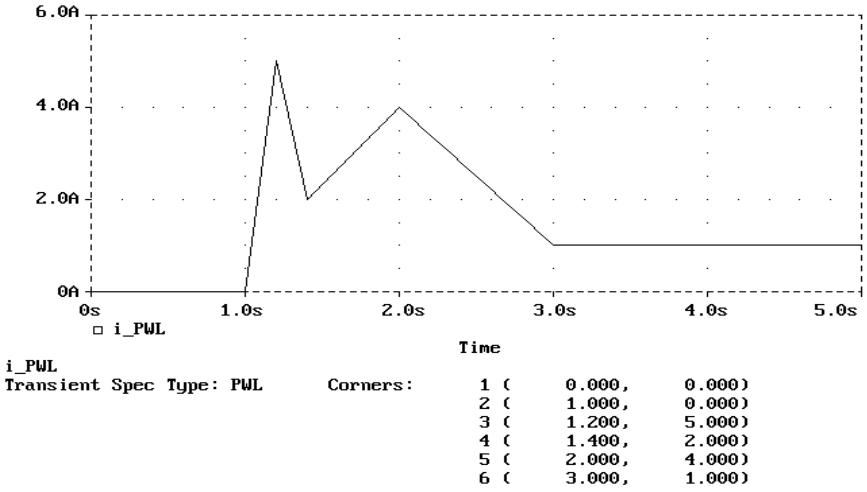
Waveform Parameters

Parameter*	Description	Units	Default
<tn>	time at corner	seconds	none
<vn>	voltage at corner	volts	none
<n>	number of repetitions	positive integer, 0, or -1	none

* <tn> and <n> cannot be expressions; <vn> may be an expression.

Description

The PWL form describes a piecewise linear waveform. Each pair of time-current values specifies a corner of the waveform. The current at times between corners is the linear interpolation of the currents at the corners.



Arguments and Options

<time_scale_factor> and/or <value_scale_factor>

Can be included immediately after the PWL keyword to show that the time and/or current value pairs are to be multiplied by the appropriate scale factor. These scale factors can be expressions, in which case they are evaluated once per outer simulation loop, and thus should be composed of expressions not containing references to voltages or currents.

<tn> and <in>

The transient specification corner points for the PWL waveform, as shown in the first example. The <in> can be an expression having the same restrictions as the scaling keywords, but <tn> must be a literal.

<file name>

The text file that supplies the time-current (<tn> <in>) pairs. The contents of this file are read by the same parser that reads the circuit file, so that engineering units (e.g., 10us) are correctly interpreted. Note that the continuation + signs in the first column are unnecessary and therefore discouraged.

A typical file can be created by editing an existing PWL specification, replacing all + signs with blanks (to avoid unintentional +time). Only numbers (with units attached) can appear in the file; expressions for <tn> and <n> values are invalid. All absolute time points in <file name> are with respect to the last (<tn> <in>) entered. All relative time points are with respect to the last time point.

REPEAT ... ENDREPEAT

These loops permit repetitions.

They can appear anywhere a (<tn> <in>) pair can appear. Absolute times within REPEAT loops are with respect to the start of the current iteration. The REPEAT ... ENDREPEAT specifications can be nested to any depth. Make sure that the current value associated with the beginning and ending time points (within the same REPEAT loop or between adjacent REPEAT loops), are the same when 0 is specified as the first point in a REPEAT loop.

<n>

`A REPEAT FOR -1 ... ENDREPEAT` is treated as if it had been `REPEAT FOREVER ... ENDREPEAT`. `A REPEAT FOR 0 ... ENDREPEAT` is ignored (other than syntax checking of the enclosed corner points).

Independent Current Source & Stimulus (SFFM)

General Form `SFFM (<ioff> <iampl> <fc> <mod> <fm>)`

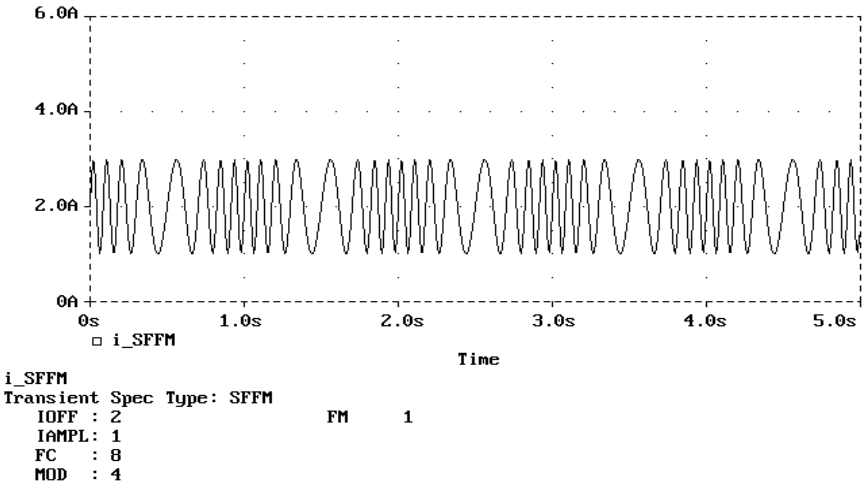
Example `IMOD 10 5 SFFM(2 1 8Hz 4 1Hz)`

Waveform Parameters

Parameters	Description	Units	Default
<ioff>	offset current	amp	none
<iampl>	peak amplitude of current	amp	none
<fc>	carrier frequency	hertz	1/TSTOP
<mod>	modulation index		0
<fm>	modulation frequency	hertz	1/**TSTOP**

Description The SFFM (Single-Frequency FM) form causes the current, as illustrated below, to follow the formula:

`ioff + iampl·sin(2p·fc·TIME + mod·sin(2p·fm·TIME) )`



Independent Current Source & Stimulus (SIN)

General Form `SIN (<ioff> <iampl> <freq> <td> <df> <phase>)`

Examples `ISIG 10 5 SIN(2 2 5Hz 1sec 1 30)`

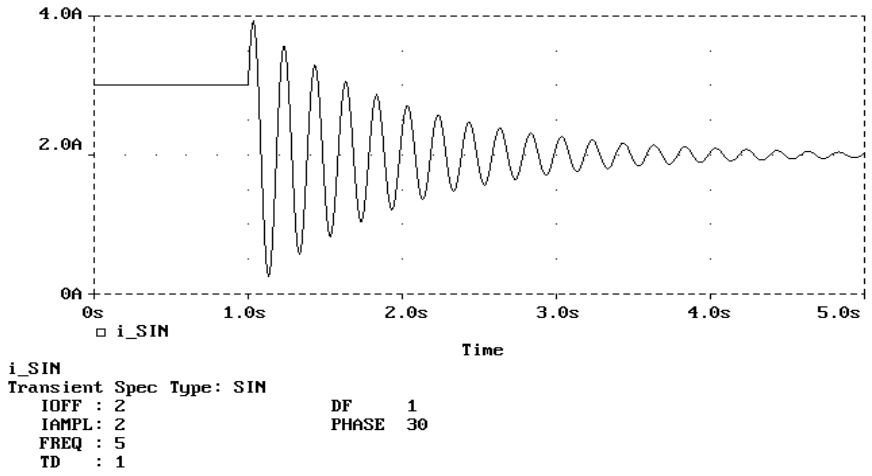
Waveform Parameters

Parameters	Description	Units	Default
<ioff>	offset current	amp	none
<iampl>	peak amplitude of current	amp	none
<freq>	frequency	hertz	1/**TSTOP**
<td>	delay	sec	0
<df>	damping factor	sec^{-1}	0
<phase>	phase	degree	0

Description

The sinusoidal (SIN) waveform causes the current to start at <ioff> and stay there for <td> seconds.

Then, the current becomes an exponentially damped sine wave. **Independent Current Source and Stimulus Sinusoidal Waveform Formulas** describe the SIN waveform.



The SIN waveform is for transient analysis only. It does not have any effect on AC analysis. To give a value to a current during AC analysis, use an AC specification, such as:

```
IAC 3 0 AC 1mA
```

where IAC has an amplitude of one milliampere during AC analysis, and can be zero during transient analysis. For transient analysis use, for example:

```
ITRAN 3 0 SIN(0 1mA 1kHz)
```

where ITRAN has an amplitude of one milliampere during transient analysis and is zero during AC analysis. Refer to your PSpice user's guide.

Independent Current Source and Stimulus Sinusoidal Waveform Formulas

Time period	Value
to <td>	ioff+iampl·*sin*(2π·phase/360°)
<td> to TSTOP	ioff+iampl·*sin*(2π·(freq·(TIME-td)+phase/360°))$e^{-(TIME-td)\cdot df}$

Inductor

General Form

```
L<name> <(+) node> <(-) node> [model name] <value>
+ [IC=<initial value>]
```

Examples

```
LLOAD 15 0 20mH
L2 1 2 .2E-6
LCHOKE 3 42 LMOD .03
LSENSE 5 12 2UH IC=2mA
```

Model Form

```
.MODEL <model name> IND [model parameters]
```

Arguments and Options

(+) and (-) nodes

Define the polarity when the inductor has a positive voltage across it.

The first node listed (or pin one in Schematics), is defined as positive. The voltage across the component is therefore defined as the first node voltage less the second node voltage.

Positive current flows from the (+) node through the inductor to the (-) node. Current flow from the first node through the component to the second node is considered positive.

[model name]

If [model name] is left out, then the effective value is <value>.

If [model name] is specified, then the effective value is given by the model parameters; see **Inductance Value Formula**.

If the inductor is associated with a Core model, then the effective value is the number of turns on the core. Otherwise, the effective value is the inductance. See the Model Form statement for the K device in **Inductor Coupling (and Magnetic Core)** for more information on the Core model.

<initial value>

Is the initial current through the inductor during the bias point calculation.

It can also be specified in a circuit file using a `.IC` statement as follows:

```
.IC I(L<name>) <initial value>
```

For details on using the .IC statement in a circuit file, see **.IC (Initial Bias Point Condition)** and refer to your PSpice user's guide for more information.

Chapter

Schematics Symbols

For standard L parts, the effective value of the part is set directly by the VALUE attribute.

In general, inductors should have positive component values (VALUE attribute). In all cases, components must not be given a value of zero.

However, there are cases when negative component values are desired. This occurs most often in filter designs that analyze an RLC circuit equivalent to a real circuit. When transforming from the real to the RLC equivalent, it is possible to end up with negative component values.

PSpice A/D allows negative component values for bias point, DC sweep, AC, and noise analyses. A transient analysis may fail for a circuit with negative components. Negative inductors may create instabilities in time that the analysis cannot handle.

Symbol Name	Model Type	Attribute	Attribute Description
L	inductor	VALUE	inductance
		IC	initial current through the inductor during bias point calculation
XFRM_LINEAR	transformer	L1_VALUE L2_VALUE	winding inductances in Henries
		COUPLING	coefficient of mutual coupling (must be between 0 and 1)
K_LINEAR	transformer	Ln	inductor reference designator

Breakout Parts

For non-stock passive and semiconductor devices, Schematics provides a set of breakout parts designed for customizing model parameters for simulation. These are useful for setting up Monte Carlo and worst-case analyses with device and/or lot tolerances specified for individual model parameters.Another approach is to use the model editor to derive an instance model and customize this. For example, you could add device and/or lot tolerances to model parameters.

Basic breakout part names consist of the intrinsic PSpice A/D device letter plus the suffix BREAK. By default, the model name is the same as the part name and references the appropriate device model with all parameters set at their default. For instance, the DBREAK part references the DBREAK model which is derived from the intrinsic PSpice A/D D model (.MODEL DBREAK D).

For breakout part LBREAK, the effective value is computed from a formula that is a function of the specified VALUE attribute.

Part Type	Symbol Name	Symbol Library File	Attribute	Description
inductor	LBREAK	`breakout.slb`	VALUE	inductance
			IC	initial current through the inductor during bias point calculation
			MODEL	IND model name

Inductor Model Parameters

Model Parameters*	Description	Units	Default
L	Inductance multiplier		1
IL1	Linear current coefficient	amp^{-1}	0
IL2	Quadratic current coefficient	amp^{-2}	0
TC1	Linear temperature coefficient	$°C^{-1}$	0
TC2	Quadratic temperature coefficient	$°C^{-2}$	0
T_ABS	Absolute temperature	°C	
T_MEASURED	Measured temperature	°C	
T_REL_GLOBAL	Relative to current temperature	°C	
T_REL_LOCAL	Relative to AKO model temperature	°C	

* For information on **T_MEASURED**, **T_ABS**, **T_REL_GLOBAL**, and **T_REL_LOCAL**, see **.MODEL (Model)**.

Inductor Equations

Inductance Value Formula

If [model name] is specified, then the effective value is given by:

$$\langle value\rangle \cdot \mathbf{L} \cdot (1+\mathbf{IL1} \cdot I+\mathbf{IL2} \cdot I^2) \cdot (1+\mathbf{TC1} \cdot (T-Tnom)+\mathbf{TC2} \cdot (T-Tnom)^2)$$

where <value> is normally positive (though it can be negative, but not zero). Tnom is the nominal temperature (set using TNOM option).

Inductor Equation for Noise

The inductor does not have a noise model.

MOSFET

General Form

```
M<name> <drain node> <gate node> <source node>
+ <bulk/substrate node> <model name>
+ [L=<value>] [W=<value>]
+ [AD=<value>] [AS=<value>]
+ [PD=<value>] [PS=<value>]
+ [NRD=<value>] [NRS=<value>]
+ [NRG=<value>] [NRB=<value>]
+ [M=<value>]
```

Examples

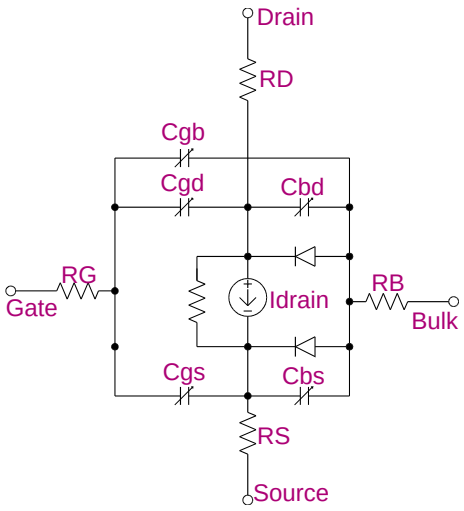
```
M1 14 2 13 0 PNOM  L=25u W=12u
M13 15 3 0 0 PSTRONG
M16 17 3 0 0 PSTRONG M=2
M28 0 2 100 100 NWEAK L=33u W=12u
+ AD=288p AS=288p PD=60u PS=60u NRD=14 NRS=24 NRG=10
```

Model Form

```
.MODEL <model name> NMOS [model parameters]
.MODEL <model name> PMOS [model parameters]
```

Description

The MOSFET is modeled as an intrinsic MOSFET using ohmic resistances in series with the drain, source, gate, and bulk (substrate). There is also a shunt resistance (RDS) in parallel with the drain-source channel.



Arguments and Options

L and W

are the channel length and width, which are decreased to get the effective channel length and width. They can be specified in the device, **.MODEL (Model)**, or **.OPTIONS (Analysis Options)** statements. The value in the device statement supersedes the value in the model statement, which supersedes the value in the .OPTIONS statement. Defaults for L and W can be set in the .OPTIONS statement. If L or W defaults are not set, their default value is 100 u.

[L=<value>] [W=<value>] cannot be used in conjunction with Monte Carlo analysis.

Chapter

AD and AS
The drain and source diffusion areas. Defaults for AD and AS can be set in the .OPTIONS statement. If AD or AS defaults are not set, their default value is 0.

PD and PS
The drain and source diffusion perimeters. Their default value is 0.

JS
Can specify the drain-bulk and source-bulk saturation currents. JS is multiplied by AD and AS.

IS
Can also specify the drain-bulk and source-bulk saturation currents. IS is an absolute value.

CJ
Can specify the zero-bias depletion capacitances. CJ is multiplied by AD and AS.

CJSW
Can also specify the zero-bias depletion capacitances. CJSW is multiplied by PD and PS.

CBD and CBS
Can also specify the zero-bias depletion capacitances. CBD and CBS are absolute values.

NRD, NRS, NRG, and NRB
Multipliers (in units of squares) that can be multiplied by RSH to yield the parasitic (ohmic) resistances of the drain (RD), source (RS), gate (RG), and substrate (RB), respectively. NRD and NRS default to 1, and NRG and NRB default to 0.

Consider a square sheet of resistive material. Analysis shows that the resistance between two parallel edges of such a sheet depends upon its composition and thickness, but is *independent* of its size as long as it is *square*. In other words, the resistance will be the same whether the square's edge is 2 mm, 2 cm, or 2 m. For this reason, the sheet resistance of such a layer, abbreviated **RSH**, has units of ohms per square.

M
A device multiplier (default = 1), which simulates the effect of multiple devices in parallel.

The effective width, overlap and junction capacitances, and junction currents of the MOSFET are multiplied by M. The parasitic resistance values (e.g., RD and RS) are divided by M. Note the third example: it shows a device twice the size of the second example.

Comments

The simulator provides six MOSFET device models, which differ in the formulation of the I-V characteristic. The **LEVEL** parameter selects between different models as follows. For more information, see **References**.

LEVEL=1	Shichman-Hodges model (see reference [1])
LEVEL=2	geometry-based, analytic model (see reference [2])
LEVEL=3	semi-empirical, short-channel model (see reference [2])
LEVEL=4	BSIM model (see reference [3])
LEVEL=5	(No longer supported.)
LEVEL=6	BSIM3 model version 2.0 (see reference [7])
LEVEL=7	BSIM3 model version 3.0 (see reference [8])

Schematics Symbols

The following table lists the set of MOSFET breakout parts designed for customizing model parameters for simulation. These are useful for setting up Monte Carlo and worst-case analyses with device and/or lot tolerances specified for individual model parameters.

Symbol Name	Model Type	Attribute	Attribute Description
MBREAKN	NMOS	L	channel length
MBREAKN3	PMOS	W	channel width
MBREAKN4		AD	drain diffusion area
MBREAKP		AS	source diffusion area
MBREAKP3		PD	drain diffusion perimeter
MBREAKP4		PS	source diffusion perimeter
		NRD	relative drain resistivity (in squares)
		NRS	relative source resistivity (in squares)
		NRG	relative gate resistivity (in squares)
		NRB	relative substrate resistivity (in squares)
		M	device multiplier (simulating parallel devices)
		MODEL	NMOS or PMOS model name

Setting operating temperature

Operating temperature can be set to be different from the global circuit temperature by defining one of the model parameters: T_ABS, T_REL_GLOBAL, or T_REL_LOCAL. Additionally, model parameters can be assigned unique measurement temperatures using the T_MEASURED model parameter. For more information, see **MOSFET Model Parameters**.

MOSFET Model Parameters

For All Model Levels

The parameters common to all model levels are primarily parasitic element values such as series resistance, overlap and junction capacitance, and so on.

Model Levels 1, 2, and 3

The DC characteristics of the first three model levels are defined by the parameters **VTO**, **KP**, **LAMBDA**, **PHI**, and **GAMMA**. These are computed by the simulator if process parameters (e.g., **TOX**, and **NSUB**) are given, but the user-specified values always override. **VTO** is positive (negative) for enhancement mode and negative (positive) for depletion mode of N-channel (P-channel) devices.

The default value for **TOX** is 0.1 μ for Levels 2 and 3, but is unspecified for Level 1, which discontinues the use of process parameters.

For MOSFETs the capacitance model has been changed to conserve charge, affecting only the Level 1, 2, and 3 models.

Effective length and width for device parameters are calculated with the formula:

$P_i = P_0 + P_L/L_e + P_W/W_e$

where:

L_e = effective length = L - (LD · 2)
W_e = effective width = W - (WD · 2)

See **.MODEL (Model)** for more information.

Model Level 4

Unlike the other models in PSpice, the BSIM model is designed for use with a process characterization system that provides all parameters. Therefore, there are no defaults specified for the parameters, and leaving one out can cause problems.

The **LEVEL**=4 (BSIM1) model parameters are all values obtained from process characterization, and can be generated automatically. Reference [4] of **References** describes a means of generating a process file, which must then be converted into **.MODEL (Model)** statements for inclusion in the Model Library or circuit file. (The simulator does not read process files.)

The level 4 (BSIM) and level 6 (BSIM3 version 2) models have their own capacitance model, which conserves charge and remains unchanged. References [6] and [7] describe the equations for the capacitance due to channel charge.

In the following **MOSFET Model Parameters** list, parameters marked with a ζ in the Default column also have corresponding parameters with a length and width dependency. For

example, VFB is a basic parameter using units of volts, and LVFB and WVFB also exist and have units of volt·µ. The formula

$P_i = P_0 + P_L/L_e + P_W/W_e$

is used to evaluate the parameter for the actual device, where:

L_e = effective length = L - DL
W_e = effective width = W - DW

Model Level 6 (BSIM3 version 2.0)

The Level 6 Advanced parameters should not be changed unless the detail structure of the device is known and has specific, meaningful values.

The BSIM3 model is a physical model using extensive built-in dependencies of important dimensional and processing parameters. It includes the major effects that are important to modeling deep-submicrometer MOSFETs, such as threshold voltage reduction, nonuniform doping, mobility reduction due to the vertical field, bulk charge effect, carrier velocity saturation, drain-induced barrier lowering (DIBL), channel length modulation (CLM), hot-carrier-induced output resistance reduction, subthreshold conduction, source/drain parasitic resistance, substrate current induced body effect (SCBE), and drain voltage reduction in LDD structure. For additional, detailed model information, see **References**.

Additional Notes

Note 1

If any of the following BSIM3 version 2.0 model parameters are not explicitly specified, they are calculated using the following equations.

$$\mathbf{VTH0} = \mathbf{VFB} + \mathbf{PHI} + \mathbf{K}\sqrt{\mathbf{PHI}}$$

$$\mathbf{K1} = \mathbf{GAMMA2} - 2 \cdot \mathbf{K2}\sqrt{(\mathbf{PHI} - \mathbf{VBM})}$$

$$\mathbf{K2} = \frac{(\mathbf{GAMMA1} - \mathbf{GAMMA2})(\sqrt{\mathbf{PHI} - \mathbf{VBX}} - \sqrt{\mathbf{PHI}})}{2\sqrt{\mathbf{PHI}}(\sqrt{\mathbf{PHI} - \mathbf{VBX}} - \sqrt{\mathbf{PHI}}) + \mathbf{VBM}}$$

$$\mathbf{VBF} = \mathbf{VTH0} - \mathbf{PHI} - \mathbf{K1}\sqrt{\mathbf{PHI}}$$

$$\mathbf{PHI} = 2V_{tm}\ln\left(\frac{\mathbf{NPEAK}}{n_i}\right)$$

$$\mathbf{GAMMA1} = \frac{\sqrt{2q\varepsilon_{si}\mathbf{NPEAK}}}{\mathbf{COX}}$$

$$\mathbf{GAMMA2} = \frac{\sqrt{2q\varepsilon_{si}\mathbf{NSUB}}}{\mathbf{COX}}$$

$$\mathbf{VBX} = \mathbf{PHI} - q \cdot \mathbf{NPEAK} \cdot \mathbf{XT}^2/(2\varepsilon_{si})$$

$$\mathbf{LITL} = \sqrt{\frac{\varepsilon_{si}\mathbf{TOX}X_j}{\varepsilon_{ox}}}$$

Note 2

Default values listed for the BSIM3 version 2.0 parameters **UA**, **UB**, **UC**, **UA1**, **AB1**, and **UC1** are used for simplified mobility modeling.

New! Model Level 7 (BSIM3 version 3.0)

The BSIM3 version 3 model is a deep submicron MOSFET model with the same physical basis as the BSIM3 version 2 model, but with a number of major enhancements, such as a single I-V expression to describe current and output conductance in all regions of device operation, better modeling of narrow width devices, a reformulated capacitance model to improve short and narrow geometry models, a new relaxation time model to improve transient modeling, and improved model fitting of various W/L ratios using one parameter set. BSIM3 version 3 retains the extensive built-in dependencies of dimensional and processing parameters of BSIM3 version 2. For additional, detailed model information, see Reference [8] of **References**.

Additional Notes

Note 1

If any of the following BSIM3 version 3.0 model parameters are not explicitly specified, they are calculated using the following equations:

If **VTHO** is not specified, then:

$$\mathbf{VTHO} = \mathbf{VFB} + \phi_s \mathbf{K1}\sqrt{\phi_s}$$

where:

VFB=-1.0

If **VTHO** is specified, then:

$$\mathbf{VFB} = \mathbf{VTHO} - \phi_s + \mathbf{K1}\sqrt{\phi_s}$$

$$\mathbf{VBX} = \phi_s - \frac{q \cdot \mathbf{NCH} \cdot XT^2}{2 \cdot \varepsilon_{si}}$$

$$\mathbf{CF} = \left(\frac{2\varepsilon_{ox}}{\pi}\right)\ln\left(1 + \frac{4 \times 10^{-7}}{\mathbf{TOX}}\right)$$

where

$E_g(T)$=the energy bandgap at temperature T= $1.16 - \frac{(7.02 \cdot 10^{-4} \cdot T^2)}{(T + 1108)}$

Note 2

If **K1** AND **K2** are not specified, they are calculated using the following equations:

$$\mathbf{K1} = \mathbf{GAMMA2} - 2\mathbf{K2}\sqrt{\phi_s - \mathbf{VBM}}$$

$$\mathbf{K2} = \frac{(\mathbf{GAMMA1} - \mathbf{GAMMA2})(\sqrt{\phi_S - \mathbf{VBX}} - \sqrt{\phi_s})}{2\sqrt{\phi_s}(\sqrt{\phi_s - \mathbf{VBM}} - \sqrt{\phi_s}) + \mathbf{VBM}}$$

where:

$$\phi_s = 2Vt \cdot \ln\left(\frac{\mathbf{NCH}}{n_i}\right)$$

$$Vt = \frac{k \cdot T}{q}$$

$$n_i = 1.45 \cdot 10^{10}\left(\frac{T}{300.15}\right)^{1.5} \qquad \exp\left(21.5565981 - \frac{E_g(T)}{2Vt}\right)$$

Note 3 If **NCH** is not given and **GAMMA1** is given, then:

$$\mathbf{NCH} = \frac{\mathbf{GAMMA1}^2 \cdot (Cox)^2}{2q \cdot \varepsilon_{si}}$$

If neither **GAMMA1** nor **NCH** is given, then **NCH** has a default value of 1.7e23 $1/m^3$ and **GAMMA1** is calculated from **NCH**:

$$\mathbf{GAMMA1} = \frac{\sqrt{2q \cdot \varepsilon_{si} \cdot \mathbf{NCH}}}{Cox}$$

If **GAMMA2** is not given, then:

$$\mathbf{GAMMA2} = \frac{\sqrt{2q \cdot \varepsilon_{si} \cdot \mathbf{NSUB}}}{Cox}$$

Note 3 If **CGSO** is not given and **DLC**>0, then:

$$\mathbf{CGSO} = (\mathbf{DLC} \cdot Cox) - \mathbf{CGS1}$$

If the previously calculated **CGSO**<0, then:

CGSO=0

Else:

CGSO=0.6 · **XJ** · Cox

Note 4 If CGDO is not given and DLC>0, then:

$$\mathbf{CGDO} = (\mathbf{DLC} \cdot Cox) - \mathbf{CGD1}$$

If the previously calculated **CGDO**<0, then

CGDO=0

Else:

CGDO=0.6 · **XJ** · Cox

MOSFET Model Parameters

Parameter*	Description	Unit	Default
	All Levels		
AF	flicker noise exponent		1
CBD	zero-bias bulk-drain *p-n* capacitance	farad	0
CBS	zero-bias bulk-source *p-n* capacitance	farad	0
CGBO	gate-bulk overlap capacitance/channel length	farad/meter	0
CGDO	gate-drain overlap capacitance/channel width	farad/meter	0
CGSO	gate-source overlap capacitance/channel width	farad/meter	0
CJ	bulk *p-n* zero-bias bottom capacitance/area	farad/meter^2	0
CJSW	bulk *p-n* zero-bias sidewall capacitance/length	farad/meter	0
FC	bulk *p-n* forward-bias capacitance coefficient		0.5
GDSNOI	channel shot noise coefficient (use with NLEV=3)		1
IS	bulk *p-n* saturation current	amp	1E-14
JS	bulk *p-n* saturation current/area	amp/meter^2	0
JSSW	bulk *p-n* saturation sidewall current/length	amp/meter	0
KF	flicker noise coefficient		0
L	channel length	meter	DEFL
LEVEL	model index		1
MJ	bulk *p-n* bottom grading coefficient		0.5
MJSW	bulk *p-n* sidewall grading coefficient		0.33
N	bulk *p-n* emission coefficient		1
NLEV	noise equation selector		2
PB	bulk *p-n* bottom potential	volt	0.8
PBSW	bulk *p-n* sidewall potential	volt	PB
RB	bulk ohmic resistance	ohm	0
RD	drain ohmic resistance	ohm	0
RDS	drain-source shunt resistance	ohm	infinite
RG	gate ohmic resistance	ohm	0
RS	source ohmic resistance	ohm	0
RSH	drain, source diffusion sheet resistance	ohm/square	0
TT	bulk p-n transit time	sec	0

MOSFET Model Parameters (continued)

Parameter*	Description	Unit	Default
T_ABS †	absolute temperature	°C	
T_MEASURED †	measured temperature	°C	
T_REL_GLOBAL †	relative to current temperature	°C	
T_REL_LOCAL †	relative to AKO model temperature	°C	
W	channel width	meter	DEFW
	Levels 1, 2, and 3		
DELTA	width effect on threshold		0
ETA	static feedback (Level 3)		0
GAMMA	bulk threshold parameter	$volt^{1/2}$	see page 2-73
KP	transconductance coefficient	$amp/volt^2$	2.0E-5
KAPPA	saturation field factor (Level 3)		0.2
LAMBDA	channel-length modulation (Levels 1 and 2)	$volt^{-1}$	0.0
LD	lateral diffusion (length)	meter	0.0
NEFF	channel charge coefficient (Level 2)		1.0
NFS	fast surface state density	$1/cm^2$	0.0
NSS	surface state density	$1/cm^2$	none
NSUB	substrate doping density	$1/cm^3$	none
PHI	surface potential	volt	0.6
THETA	mobility modulation (Level 3)	$volt^{-1}$	0.0
TOX	oxide thickness	meter	see page 2-73
TPG	Gate material type: +1 = opposite of substrate -1 = same as substrate 0 = aluminum		+1
UCRIT	mobility degradation critical field (Level 2)	volt/cm	1.0E4
UEXP	mobility degradation exponent (Level 2)		0.0
UTRA	(not used) mobility degradation transverse field coefficient		0.0
UO	surface mobility (The second character is the letter O, not the numeral zero.)	$cm^2/volt \cdot sec$	600
VMAX	maximum drift velocity	meter/sec	0

MOSFET Model Parameters (continued)

Parameter*	Description	Unit	Default
VTO	zero-bias threshold voltage	volt	0
WD	lateral diffusion (width)	meter	0
XJ	metallurgical junction depth (Levels 2 and 3)	meter	0
XQC	fraction of channel charge attributed to drain		1.0
	Level 4**		
DL	Channel shortening	m	
DW	Channel narrowing	m	
ETA	Zero-bias drain-induced barrier lowering coefficient		ζ
K1	Body effect coefficient	$volt^{1/2}$	ζ
K2	Drain/source depletion charge sharing coefficient		ζ
MUS	Mobility at zero substrate bias and Vds=Vdd	$cm^2/volt^2 \cdot sec$	ζ
MUZ	Zero-bias mobility	$cm^2/volt \cdot sec$	
N0	Zero-bias subthreshold slope coefficient		ζ
NB	Sens. of subthreshold slope to substrate bias		ζ
ND	Sens. of subthreshold slope to drain bias		ζ
PHI	Surface inversion potential	volt	ζ
TEMP	Temperature at which parameters were measured	°C	
TOX	Gate-oxide thickness	m	
U0	Zero-bias transverse-field mobility degradation	$volt^{-1}$	ζ
U1	Zero-bias velocity saturation	µ/volt	ζ
VDD	Measurement bias range	volts	
VFB	Flat-band voltage	volt	ζ
WDF	Drain, source junction default width	meter	
X2E	Sens. of drain-induced barrier lowering effect to substrate bias	$volt^{-1}$	ζ
X2MS	Sens. of mobility to substrate bias @ Vds=0	$cm^2/volt^2 \cdot sec$	ζ
X2MZ	Sens. of mobility to substrate bias @ Vds=0	$cm^2/volt^2 \cdot sec$	ζ
X2U0	Sens. of transverse-field mobility degradation effect to substrate bias	$volt^{-2}$	ζ
X2U1	Sens. of velocity saturation effect to substrate bias	$µ/volt^2$	ζ

MOSFET Model Parameters (continued)

Parameter*	Description	Unit	Default
X3E	Sens. of drain-induced barrier lowering effect to drain bias @ Vds = Vdd	$volt^{-1}$	ζ
X3MS	Sens. of mobility to drain bias @ Vds=Vdd	$cm^2/volt^2 \cdot sec$	ζ
X3U1	Sens. of velocity saturation effect on drain	$\mu/volt^2$	ζ
XPART	Gate-oxide capacitance charge model flag. **XPART**=0 selects a 40/60 drain/source charge partition in saturation, while **XPART**=1 selects a 0/100 drain/source charge partition.		
	Level 6		
A0	bulk charge effect coefficient NMOS		1.0
	bulk charge effect coefficient PMOS		4.4
A1	first non-saturation coefficient NMOS	1/V	0.0
	first non-saturation coefficient PMOS	1/V	0.23
A2	second non-saturation coefficient NMOS		1.0
	second non-saturation coefficient PMOS		0.08
AT	saturation velocity temperature coefficient	m/sec	3.3E4
BULKMOD	bulk charge model selector:		
	NMOS		1
	PMOS		2
CDSC	drain/source and channel coupling capacitance	F/m^2	2.4E-4
CDSCB	body bias sensitivity of CDSC	F/Vm^2	0.0
DL	channel length reduction on one side	m	0.0
DROUT	channel length dependent coefficient of the DIBL effect on Rout		0.56
DSUB	subthreshold DIBL coefficient exponent		DROUT
DVT0	first coefficient of short-channel effect on threshold voltage		2.2
DVT1	second coefficient of short-channel effect on threshold voltage		0.53

MOSFET Model Parameters (continued)

Parameter*	Description	Unit	Default
DVT2	body bias coefficient of short-channel effect on threshold voltage	1/V	-0.032
DW	channel width reduction on one side	m	0.0
ETA0	DIBL coefficient in subthreshold region		0.08
ETAB	body bias coefficient for the subthreshold DIBL coefficient	1/V	-0.07
K1	first-order body effect coefficient	$\sqrt{V}$	see page 2-74
K2	second-order body effect coefficient		see page 2-74
K3	narrow width effect coefficient		80.0
K3B	body effect coefficient of K3	1/V	0.0
KETA	body bias coefficient of the bulk charge effect.	1/V	-0.047
KT1	temperature coefficient for threshold voltage	V	-0.11
KT1L	channel length sensitivity of temperature coefficient for threshold voltage.	V-m	0.0
KT2	body bias coefficient of the threshold voltage temperature effect		0.022
NFACTOR	subthreshold swing coefficient		1.0
NGATE	poly gate doping concentration	$1/cm^3$	
NLX	lateral nonuniform doping coefficient	m	1.74E-7
NPEAK	peak doping concentration near interface	$1/cm^3$	1.7E17
NSUB	substrate doping concentration	$1/cm^3$	6.0E16
PCLM	channel length modulation coefficient		1.3
PDIBL1	first output resistance DIBL effect coefficient		0.39
PDIBL2	second output resistance DIBL effect coefficient		0.0086
PSCBE1	first substrate current body effect coefficient	V/m	4.24E8
PSCBE2	second substrate current body effect coefficient	m/V	1.0E-5
PVAG	gate dependence of Early voltage		0.0
RDS0	contact resistance	ohms	0.0
RDSW	parasitic resistance per unit width	ohms/ μm	0.0

MOSFET Model Parameters (continued)

Parameter*	Description	Unit	Default
SATMOD	saturation model selector: For semi-empirical output: resistance model 1 For physical output: resistance model 2		2
SUBTHMOD	subthreshold model selector: no subthreshold model 0 BSIM1 subthreshold model 1 BSIM3 subthreshold model 2 BSIM3 subthreshold model using log current 3		2
TNOM	temperature at which parameters are extracted.	deg. C	27
TOX	gate oxide thickness	m	1.5E-8
UA	first-order mobility degradation coefficient	m/V	2.25E-9
UA1	temperature coefficient for **UA**	m/V	4.31E-9
UB	second-order mobility degradation coefficient	$(m/V)^2$	5.87E-19
UB1	temperature coefficient for **UB**	$(m/V)^2$	-7.61E-18
UC	body effect mobility degradation coefficient	1/V	0.0465
UC1	temperature coefficient for **UC**	1/V	-0.056
UTE	mobility temperature exponent		-1.5
VOFF	offset voltage in subthreshold region	V	-0.11
VSAT	saturation velocity at Temp=**TNOM**	cm/sec	8.0E6
VTH0	threshold voltage at Vbs=0 for large channel length	V	see page 2-74
W0	narrow width effect parameter	m	2.5E-6
XJ	junction depth	m	1.5E-7
XPART	charge partitioning coefficient: no charge model < 0.0 40/60 partition = 0.0 50/50 partition = 0.5 0/100 partition = 1.0		0.0

MOSFET Model Parameters (continued)

Parameter*	Description	Unit	Default
	Level 6 Advanced		
CIT	capacitance due to interface trapped charge	F/m^2	0.0
EM	critical electrical field in channel	V/m	4.1E7
ETA	drain voltage reduction coefficient due to LDD		0.3
GAMMA1	body effect coefficient near the interface	$\sqrt{V}$	see page 2-74
GAMMA2	body effect coefficient in the bulk	$\sqrt{V}$	see page 2-74
LDD	total length of the LDD region	m	0.0
LITL	characteristic length related to current depth	m	see page 2-74
PHI	surface potential under strong inversion	V	see page 2-74
U0	mobility at Temp=TNOM:		
	NMOS	$cm^2/V\text{-}sec$	670.0
	PMOS	$cm^2/V\text{-}sec$	250.0
VBM	maximum applied body bias	V	-5.0
VBX	vbs at which the depletion width equals XT	V	see page 2-74
VFB	flat-band voltage	V	see page 2-74
VGHIGH	voltage shift of the higher bound of the transition region	V	0.12
VGLOW	voltage shift of the lower bound of the transition region	V	-0.12
XT	doping depth	m	1.55E-7
	Level 7: Control Parameters		
CAPMOD	flag for the short-channel capacitance model	none	1
MOBMOD	mobility model selector	none	1
NOIMOD	flag for noise model	none	1
NQSMOD	flag for NQS model	none	0

MOSFET Model Parameters (continued)

Parameter*	Description	Unit	Default
	Level 7: AC and Capacitance Parameters		
CF	fringing field capacitance	F/m	see page 2-75
CKAPPA	coefficient for lightly doped region overlap capacitance fringing field capacitance	F/m	0.6
CLC	constant term for the short-channel model	m	1.0E-6
CLE	exponential term for the short-channel model	none	0.6
CGBO	gate bulk overlap capacitance per unit channel length	F/m	0.0
CGD1	light-doped drain-gate region overlap capacitance	F/m	0.0
CGDO	non-LDD region drain-gate overlap capacitance per channel length	F/m	see page 2-75
CGS1	light-doped source-gate region overlap capacitance	F/m	0.0
CGSO	non-LDD region source-gate overlap capacitance per channel length	F/m	see page 2-75
CJ	bottom junction per unit area	F/m^2	5.0E-4
CJSW	source/drain side junction capacitance per unit area	F/m^2	5.0E-10
DLC	length offset fitting parameter from C-V	m	LINT
DWC	width offset fitting parameter from C-V	m	WINT
MJ	bottom junction capacitance grading coefficient	none	0.5
MJSW	source/drain side junction capacitance grading coefficient	none	0.33
PB	bottom built-in potential	V	1.0
PBSW	source/drain side junction built-in potential	V	1.0
XPART	charge partitioning rate flag	none	0.0
	Level 7: Bin Description Parameters		
BINUNIT	bin unit scale selector	none	1.0
LMAX	maximum channel length	m	1.0
LMIN	minimum channel length	m	0.0
WMAX	maximum channel width	m	1.0
WMIN	minimum channel width	m	0.0

MOSFET Model Parameters (continued)

Parameter*	Description	Unit	Default
	Level 7: DC Parameters		
A0	bulk charge effect coefficient for channel length	none	1.0
A1	first non-saturation effect parameter	1/V	0.0
A2	second non-saturation factor	none	1.0
AGS	gate-bias coefficient of Abulk	1/V	0.0
ALPHA0	first parameter of impact-ionization current	m/V	0.0
B0	bulk charge effect coefficient for channel width	m	0.0
B1	bulk charge effect width offset	m	0.0
BETA0	second parameter of impact-ionization current	V	30.0
CDSC	drain/source to channel coupling capacitance	F/m^2	2.4E-4
CDSCB	body-bias sensitivity of **CDSC**	F/Vm^2	0.0
CDSCD	drain-bias sensitivity of **CDSC**	F/Vm^2	0.0
CIT	interface trap capacitance	F/m^2	0.0
DELTA	effective Vds parameter	V	0.01
DROUT	L-dependence coefficient of the DIBL correction parameter in Rout	none	0.56
DSUB	dibl coefficient exponent in subthreshold region	none	**DROUT**
DVT0	first coefficient of short-channel effect on threshold voltage	none	2.2
DVT0W	first coefficient of narrow-width effect on threshold voltage for small-channel length	1/m	0.0
DVT1	second coefficient of short-channel effect on threshold voltage	none	0.53
DVT2	body-bias coefficient of short-channel effect on threshold voltage	1/V	-0.032
DVTW1	second coefficient of narrow-width effect on threshold voltage for small channel length	1/m	5.3E6
DVTW2	body-bias coefficient of narrow-width effect for small channel length	1/V	-0.032
DWB	coefficient of substrate body bias dependence of Weff	$m/V^{1/2}$	0.0
DWG	coefficient of gate dependence of Weff	m/V	0.0

MOSFET Model Parameters (continued)

Parameter*	Description	Unit	Default
ETA0	DIBL coefficient in subthreshold region	none	0.08
ETAB	body-bias coefficient for the subthreshold DIBL effect	1/V	-0.07
JS	source-drain junction saturation current per unit area	A/m^2	1.0E-4
K1	first-order body effect coefficient	$V^{1/2}$	0.5 see page 2-75
K2	second-order body effect coefficient	none	0.0 see page 2-75
K3	narrow width coefficient	none	80.0
K3B	body effect coefficient of **K3**	1/V	0.0
KETA	body-bias coefficient of bulk charge effect	1/V	-0.047
LINT	length offset fitting parameter from I-V without bias	m	0.0
NFACTOR	subthreshold swing factor	none	1.0
NGATE	poly gate doping concentration	cm^{-3}	infinite
NLX	lateral non-uniform doping parameter	m	1.74E-7
PCLM	channel length modulation parameter	none	1.3
PDIBLC1	first output resistance DIBL effect correction parameter	none	0.39
PDIBLC2	second output resistance DIBL effect correction parameter	none	0.0086
PDIBLCB	body effect coefficient of DIBL correction parameter	1/V	0.0
PRWB	body-effect coefficient of **RDSW**	$1/V^{1/2}$	0.0
PRWG	gate bias effect coefficient of **RDSW**	1/V	0.0
PSCBE1	first substrate current body-effect parameter	V/m	4.24E8
PSCBE2	second substrate current body-effect parameter	V/m	1.0E-5
PVAG	gate dependence of Early voltage	none	0.0
RDSW	parasitic resistance per unit width	Ω-μm^{WR}	0.0
RSH	source-drain sheet resistance	Ω/square	0.0

MOSFET Model Parameters (continued)

Parameter*	Description	Unit	Default
U0	mobility at Temp=**TNOM** NMOS PMOS	 670.0 250.0	 $cm^2/(V \cdot sec)$
UA	first-order mobility degradation coefficient	m/V	2.25E-9
UB	second-order mobility degradation coefficient	$(m/V)^2$	5.87E-19
UC	body-effect of mobility degradation coefficient	m/V^2	-4.65E-11 when **MOBMOD**=1 or 2
		1/V	-0.046 when **MOBMOD**=3
VBM	maximum applied body bias in threshold voltage calculation	V	-5.0
VOFF	offset voltage in the subthreshold region at large W and L	V	-0.08
VSAT	saturation velocity at Temp=**TNOM**	m/sec	8.0E 4
VTH0	threshold voltage@Vbs=0 for large L	V	0.7 (NMOS) -0.7 (PMOS) see page 2-75
W0	narrow-width parameter	m	2.5E-6
WINT	width-offset fitting parameter from I-V without bias	m	0.0
WR	width offset from Weff for Rds calculation	none	1.0
	Level 7: Flicker Noise Parameters		
AF	frequency exponent	none	1.0
EF	flicker exponent for **NOIMOD**=2	none	1.0
EM	saturation field	V/m	4.1E7
KF	flicker noise parameter for **NOIMOD**=1	none	0.0
NOIA	noise parameter A	none	1.0E20 (NMOS) 9.9E18 (PMOS)
NOIB	noise parameter B	none	5.0E4 (NMOS) 2.4E3 (PMOS)
NOIC	noise parameter C	none	-1.4E-12 (NMOS) 1.4E-12 (PMOS)

MOSFET Model Parameters (continued)

Parameter*	Description	Unit	Default
	Level 7: NQS Parameter		
ELM	Elmore constant of the channel	none	5.0
	Level 7: Process Parameters		
GAMMA1	body-effect coefficient near the surface	$V^{1/2}$	see page 2-75
GAMMA2	body-effect coefficient in the bulk	$V^{1/2}$	see page 2-75
NCH	channel doping concentration	$1/cm^3$	1.7E17
NSUB	substrate doping concentration	$1/cm^3$	6.0E16
TOX	gate-oxide thickness	m	1.5E-8
VBX	Vbs at which the depletion region = **XT**	V	see page 2-75
XJ	junction depth	m	1.5E-7
XT	doping depth	m	1.55E-7
	Level 7: Temperature Parameters		
AT	temperature coefficient for saturation velocity	m/sec	3.3E4
KT1	temperature coefficient for threshold voltage	V	-0.11
KT1L	channel length dependence of the temperature coefficient for threshold voltage	V*m	0.0
KT2	body-bias coefficient of threshold voltage temperature effect	none	0.022
PRT	temperature coefficient for **RDSW**	Ω-µm	0.0
TNOM	temperature at which parameters are extracted	°C	27.0
UA1	temperature coefficient for **UA**	m/V	4.31E-9
UB1	temperature coefficient for **UB**	$(m/V)^2$	-7.61E-18
UC1	temperature coefficient for **UC**	m/V^2	-5.6E -11 when **MOBMOD**=1 or 2
		1/V	-0.056 when **MOBMOD**=3
UTE	mobility temperature exponent	none	-1.5

MOSFET Model Parameters (continued)

Parameter*	Description	Unit	Default
	Level 7: W and L Parameters		
LL	coefficient of length dependence for length offset	m^{LLN}	0.0
LLN	power of length dependence for length offset	none	1.0
LW	coefficient of width dependence for length offset	m^{LWN}	0.0
LWL	coefficient of length and width cross term for length offset	$m^{LWN+LLN}$	0.0
LWN	power of width dependence for length offset	none	1.0
WL	coefficient of length dependence for width offset	m^{WLN}	0.0
WLN	power of length dependence of width offset	none	1.0
WW	coefficient of width dependence for width offset	m^{WWN}	0.0
WWL	coefficient of length and width cross term for width offset	$m^{WWN+WLN}$	0.0
WWN	power of width dependence of width offset	none	1.0

* See **.MODEL (Model)**.

A ζ in the Default column indicates that the parameter may have corresponding parameters exhibiting length and width dependence. See **Model Level 4.

† For information on **T_MEASURED**, **T_ABS**, **T_REL_GLOBAL**, and **T_REL_LOCAL**, see **.MODEL (Model)**.

MOSFET Equations

These equations describe an N-channel MOSFET. For P-channel devices, reverse the signs of all voltages and currents.

In the following equations:

Vbs	= intrinsic substrate-intrinsic source voltage
Vbd	= intrinsic substrate-intrinsic drain voltage
Vds	= intrinsic drain-intrinsic source voltage
Vdsat	= saturation voltage
Vgs	= intrinsic gate-intrinsic source voltage
Vgd	= intrinsic gate-intrinsic drain voltage
Vt	= $k \cdot T/q$ (thermal voltage)
Vth	= threshold voltage
C_{ox}	= the gate oxide capacitance per unit area.
f	= noise frequency
k	= Boltzmann's constant
q	= electron charge
Leff	= effective channel length
Weff	= effective channel width
T	= analysis temperature (°K)
Tnom	= nominal temperature (set using TNOM option)

Other variables are from **MOSFET Model Parameters**.

Positive current is current flowing into a terminal (for example, positive drain current flows from the drain through the channel to the source).

MOSFET Equations for DC Current

All Levels

Ig = gate current = 0

Ib = bulk current = Ibs+Ibd

where

Ibs = bulk-source leakage current = $Iss \cdot (e^{Vbs/(N \cdot Vt)} - 1)$

Ibd = bulk-drain leakage current = $Ids \cdot (e^{Vbd/(N \cdot Vt)} - 1)$

where
if
JS = 0, or AS = 0, or AD = 0

then
Iss = IS
Ids = IS

else
Iss = AS·**JS** + PS·**JSSW**
Ids = AD·**JS** + PD·**JSSW**

Id = drain current = Idrain-Ibd

Is = source current = -Idrain-Ibs

Level 1: Idrain

Normal Mode: Vds > 0

Case 1

for cutoff region: $Vgs - V_{to} < 0$

then: Idrain = 0

Case 2

for linear region: $Vds < Vgs - V_{to}$

then: $Idrain = (W/L) \cdot (\mathbf{KP}/2) \cdot (1 + \mathbf{LAMBDA} \cdot Vds) \cdot Vds \cdot (2 \cdot (Vgs - V_{to}) - Vds)$

Case 3

for saturation region: $0 \le Vgs - V_{to} \le Vds$

then: $Idrain = (W/L) \cdot (\mathbf{KP}/2) \cdot (1 + \mathbf{LAMBDA} \cdot Vds) \cdot (Vgs - V_{to})^2$

where
$V_{to} = \mathbf{VTO} + \mathbf{GAMMA} \cdot ((\mathbf{PHI} - Vbs)^{1/2} - \mathbf{PHI}^{1/2})$

Inverted Mode: Vds < 0

Switch the source and drain in the equations above.

Levels 2 and 3: Idrain

See reference [2] of **References** for detailed information.

MOSFET Equations for Capacitance

All capacitances are between terminals of the intrinsic MOSFET, that is, to the inside of the ohmic drain and source resistances. For Levels 1, 2, and 3, the capacitance model has been changed to conserve charge.

Levels 1, 2, and 3

Cbs = bulk-source capacitance = area cap. + sidewall cap. + transit time cap.

Cbd = bulk-drain capacitance = area cap. + sidewall cap. + transit time cap.

where
if
CBS = 0 *AND* **CBD** = 0

then
Cbs = AS·**CJ**·Cbsj + PS·**CJSW**·Cbss + **TT**·Gbs
Cbd = AD·**CJ**·Cbdj + PD·**CJSW**·Cbds + **TT**·Gds

else
Cbs = **CBS**·Cbsj + PS·**CJSW**·Cbss + **TT**·Gbs
Cbd = **CBD**·Cbdj + PD·**CJSW**·Cbds + **TT**·Gds
where
Gbs = DC bulk-source conductance = *d*Ibs/*d*Vbs
Gbd = DC bulk-drain conductance = *d*Ibd/*d*Vbd

if
Vbs ≤ **FC**·**PB**

then
Cbsj = $(1\text{-Vbs}/\mathbf{PB})^{-MJ}$
Cbss = $(1\text{-Vbs}/\mathbf{PBSW})^{-MJSW}$

if
Vbs > **FC**·**PB**

then
Cbsj = $(1\text{-}\mathbf{FC})^{-(1+MJ)}\cdot(1\text{-}\mathbf{FC}\cdot(1+\mathbf{MJ})+\mathbf{MJ}\cdot\text{Vbs}/\mathbf{PB})$
Cbss = $(1\text{-}\mathbf{FC})^{-(1+MJSW)}\cdot(1\text{-}\mathbf{FC}\cdot(1+\mathbf{MJSW})+\mathbf{MJSW}\cdot\text{Vbs}/\mathbf{PBSW})$

if
Vbd ≤ **FC**·**PB**

then
Cbdj = $(1\text{-Vbd}/\mathbf{PB})^{-MJ}$
Cbds = $(1\text{-Vbd}/\mathbf{PBSW})^{-MJSW}$

if
Vbd > **FC**·**PB**

then
Cbdj = $(1\text{-}\mathbf{FC})^{-(1+\mathbf{MJ})}\cdot(1\text{-}\mathbf{FC}\cdot(1+\mathbf{MJ})+\mathbf{MJ}\cdot\text{Vbd}/\mathbf{PB})$
Cbds = $(1\text{-}\mathbf{FC})^{-(1+\mathbf{MJSW})}\cdot(1\text{-}\mathbf{FC}\cdot(1+\mathbf{MJSW}))$

Cgs = gate-source overlap capacitance = **CGSO**·W

Cgd = gate-drain overlap capacitance = **CGDO**·W

Cgb = gate-bulk overlap capacitance = **CGBO**·L

Levels 4 and 6

See references [6] and [7] of **References**.

MOSFET Equations for Temperature Effects

The ohmic (parasitic) resistances have no temperature dependence.

All Levels

IS(T) = **IS**·$e^{(Eg(Tnom)\cdot T/Tnom - Eg(T))/Vt}$

JS(T) = **JS**·$e^{(Eg(Tnom)\cdot T/Tnom - Eg(T))/Vt}$

JSSW(T) = **JSSW**·$e^{(Eg(Tnom)\cdot T/Tnom - Eg(T))/Vt}$

PB(T) = **PB**·T/Tnom - 3·Vt·*ln*(T/Tnom) - Eg(Tnom)·T/Tnom + Eg(T)

PBSW(T) = **PBSW**·T/Tnom - 3·Vt·*ln*(T/Tnom) - Eg(Tnom)·T/Tnom + Eg(T)

PHI(T) = **PHI**·T/Tnom - 3·Vt·*ln*(T/Tnom) - Eg(Tnom)·T/Tnom + Eg(T)

where

Eg(T) = silicon bandgap energy = 1.16 - .000702·T^2/(T+1108)

CBD(T) = **CBD**·(1+**MJ**·(.0004·(T-Tnom)+(1-**PB**(T)/**PB**)))

CBS(T) = **CBS**·(1+**MJ**·(.0004·(T-Tnom)+(1-**PB**(T)/**PB**)))

CJ(T) = **CJ**·(1+**MJ**·(.0004·(T-Tnom)+(1-**PB**(T)/**PB**)))

CJSW(T) = **CJSW**·(1+**MJSW**·(.0004·(T-Tnom)+(1-**PB**(T)/**PB**)))

KP(T) = **KP**·$(T/Tnom)^{3/2}$

UO(T) = **UO**·$(T/Tnom)^{-3/2}$

MUS(T) = **MUS**·$(T/Tnom)^{-3/2}$

MUZ() = **MUZ**·$(T/Tnom)^{-3/2}$

X3MS(T) = **X3MS**·$(T/Tnom)^{-3/2}$

MOSFET Equations for Noise

Noise is calculated assuming a 1.0-hertz bandwidth, using the following spectral power densities (per unit bandwidth).

The model parameter **NLEV** is used to select the form of shot and flicker noise, and **GDSNOI** is the channel shot noise coefficient model parameter. When **NLEV**<3, the original SPICE2 shot noise equation is used in both the linear and saturation regions, but the use of this equation may produce inaccurate results in the linear region. When **NLEV**=3, a different equation is used that is valid in both linear and saturation regions.

The model parameters **AF** and **KF** are used in the small-signal AC noise analysis to determine the equivalent MOSFET flicker noise.

For more information, see reference [5] of **References**.

MOSFET Channel Shot and Flicker Noise

$$Ichan^2 = Ishot^2 + Iflick^2$$

Intrinsic MOSFET Flicker Noise

for **NLEV** = 0

$$Iflick^2 = \frac{\mathbf{KF} \cdot Idrain^{\mathbf{AF}}}{COX \cdot Leff^2 \cdot f}$$

for **NLEV** = 1

$$Iflick^2 = \frac{\mathbf{KF} \cdot Idrain^{\mathbf{AF}}}{COX \cdot Weff \cdot Leff \cdot f}$$

for **NLEV** = 2, **NLEV** = 3

$$Iflick^2 = \frac{\mathbf{KF} \cdot gm^2}{COX \cdot Weff \cdot Leff \cdot f^{\mathbf{AF}}}$$

Intrinsic MOSFET Shot Noise

for **NLEV** < 3

$$Ishot^2 = \frac{8 \cdot k \cdot T \cdot gm}{3}$$

for **NLEV** = 3

$$Ishot^2 \equiv \frac{8 \cdot k \cdot T}{3} \times \beta \times (Vgs - Vth) \frac{1 + a + a^2}{1 + a} \times \mathbf{GDSNOI}$$

where
for linear region:
$a = 1 - (Vds/Vdsat)$
for saturation region:
$a = 0$

Parasitic Resistance Thermal Noise

RD $Id^2 = 4 \cdot k \cdot T/RD$

RG $Ig^2 = 4 \cdot k \cdot T/RG$

RS $Is^2 = 4 \cdot k \cdot T/RS$

RB $Ib^2 = 4 \cdot k \cdot T/RB$

References

For a more complete description of the MOSFET models, refer to:

[1] H. Shichman and D. A. Hodges, “Modeling and simulation of insulated-gate field-effect transistor switching circuits,” IEEE Journal of Solid-State Circuits, SC-3, 285, September 1968.

[2] A. Vladimirescu, and S. Lui, “The Simulation of MOS Integrated Circuits Using SPICE2,” Memorandum No. M80/7, February 1980.

[3] B. J. Sheu, D. L. Scharfetter, P.-K. Ko, and M.-C. Jeng, “BSIM: Berkeley Short-Channel IGFET Model for MOS Transistors,” IEEE Journal of Solid-State Circuits, SC-22, 558-566, August 1987.

[4] J. R. Pierret, “A MOS Parameter Extraction Program for the BSIM Model,” Memorandum No. M84/99 and M84/100, November 1984.]

[5] P. Antognetti and G. Massobrio, Semiconductor Device Modeling with SPICE, McGraw-Hill, 1993.

[6] Ping Yang, Berton Epler, and Pallab K. Chatterjee, “An Investigation of the Charge Conservation Problem for MOSFET Circuit Simulation,” IEEE Journal of Solid-State Circuits, Vol. SC-18, No.1, February 1983.

[7] J.H. Huang, Z.H. Liu, M.C. Jeng, K. Hui, M. Chan, P.K. KO, and C. Hu, “BSIM3 Manual,” Department of Electrical Engineering and Computer Science, University of California, Berkeley, CA 94720.

[8] Department of Electrical Engineering and Computer Science, “BSIM3v3 Manual (Final version),” University of California, Berkeley CA 94720.

[9] J. C. Bowers, and H. A. Neinhaus, SPICE2 Computer Models for HEXFETs, Application Note 954A, reprinted in HEXFET Power MOSFET Databook, International Rectifier Corporation #HDB-3.

For more information on References [2] and [4], contact:

Software Distribution Office
EECS/ERL Industrial Liaison Program
205 Cory Hall #1770
University of California
Berkeley, CA 94720-1770
(510) 643-6687

Bipolar Transistor

General Form

```
Q<name> < collector node> <base node> <emitter node>
+ [substrate node] <model name> [area value]
```

Examples

```
Q1 14 2 13 PNPNOM
Q13 15 3  0 1 NPNSTRONG 1.5
Q7 VC 5 12 [SUB] LATPNP
```

Model Form

```
.MODEL <model name> NPN [model parameters]
.MODEL <model name> PNP [model parameters]
.MODEL <model name> LPNP [model parameters]
```

Arguments and Options

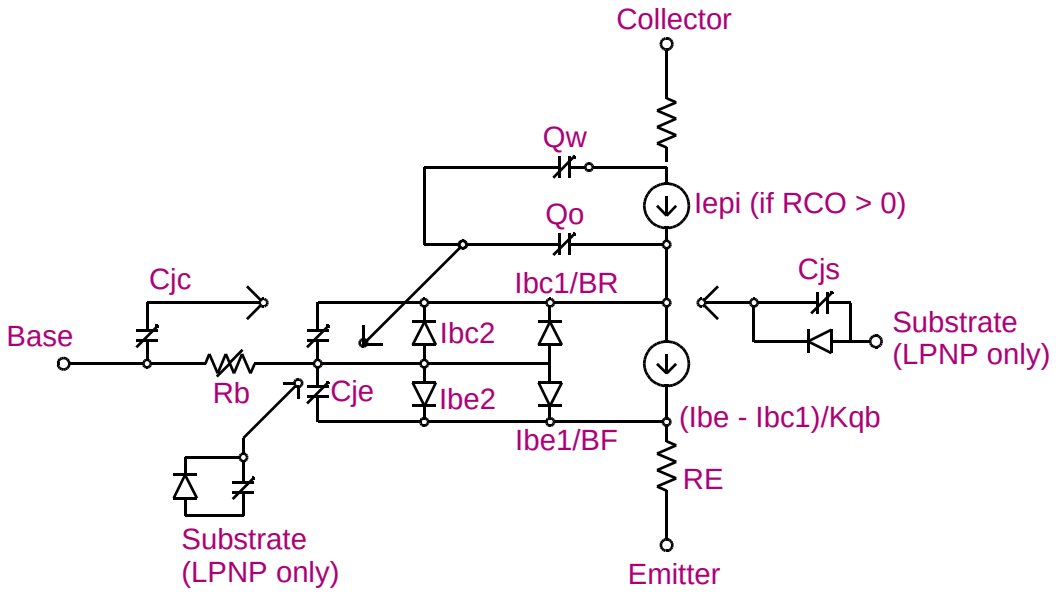
[substrate node]
is optional, and if not specified, the default is the ground.

Because the simulator allows alphanumeric names for nodes, and because there is no easy way to distinguish these from the model names, the name (not a number) used for the substrate node needs to be enclosed with square brackets [ ]. Otherwise, nodes would be interpreted as model names. See the third example.

[area value]
is the relative device area and has a default value of 1.

Description

The bipolar transistor is modeled as an intrinsic transistor using ohmic resistances in series with the collector (**RC**/area), with the base (value varies with current, see **Bipolar Transistor Equations**), and with the emitter (**RE**/area).



Positive current is current flowing into a terminal.

Chapter

For model parameters with alternate names, such as **VAF** and **VA** (the alternate name is shown by using parentheses), either name can be used.

For model types NPN and PNP, the isolation junction capacitance is connected between the intrinsic-collector and substrate nodes. This is the same as in SPICE2, or SPICE3, and works well for vertical IC transistor structures. For lateral IC transistor structures there is a third model, LPNP, where the isolation junction capacitance is connected between the intrinsic-base and substrate nodes.

Schematics Symbols

The following table lists the set of bipolar transistor breakout parts designed for customizing model parameters for simulation. These are useful for setting up Monte Carlo and worst-case analyses with device and/or lot tolerances specified for individual model parameters.

Symbol Name	Model Type	Attribute	Attribute Description
QBREAKL	LPNP	AREA MODEL	area scaling factor LNP model name
QBREAKN QBREAKN3 QBREAKN4	NPN	AREA MODEL	area scaling factor NPN model name
QBREAKP QBREAKP3 QBREAKP4	PNP	AREA MODEL	area scaling factor PNP model name

Setting operating temperature

Operating temperature can be set to be different from the global circuit temperature by defining one of the model parameters: T_ABS, T_REL_GLOBAL, or T_REL_LOCAL. Additionally, model parameters can be assigned unique measurement temperatures using the T_MEASURED model parameter. See **Bipolar Transistor Model Parameters** for more information.

Bipolar Transistor Model Parameters

Model Parameters*	Description	Units	Default
AF	flicker noise exponent		1.0
BF	ideal maximum forward beta		100.0
BR	ideal maximum reverse beta		1.0
CJC	base-collector zero-bias p-n capacitance	farad	0.0
CJE	base-emitter zero-bias p-n capacitance	farad	0.0
CJS (CCS)	substrate zero-bias p-n capacitance	farad	0.0
EG	bandgap voltage (barrier height)	eV	1.11
FC	forward-bias depletion capacitor coefficient		0.5
GAMMA	epitaxial region doping factor		1E-11
IKF (IK)	corner for forward-beta high-current roll-off	amp	infinite
IKR	corner for reverse-beta high-current roll-off	amp	infinite
IRB	current at which Rb falls halfway to	amp	infinite
IS	transport saturation current	amp	1E-16
ISC (C4) †	base-collector leakage saturation current	amp	0.0
ISE (C2) †	base-emitter leakage saturation current	amp	0.0
ISS	substrate p-n saturation current	amp	0.0
ITF	transit time dependency on Ic	amp	0.0
KF	flicker noise coefficient		0.0
MJC (MC)	base-collector p-n grading factor		0.33
MJE (ME)	base-emitter p-n grading factor		0.33
MJS (MS)	substrate p-n grading factor		0.0
NC	base-collector leakage emission coefficient		2.0
NE	base-emitter leakage emission coefficient		1.5
NF	forward current emission coefficient		1.0
NK	high-current roll-off coefficient		0.5
NR	reverse current emission coefficient		1.0
NS	substrate p-n emission coefficient		1.0
PTF	excess phase @ $1/(2\pi \cdot TF)$Hz	degree	0.0
QCO	epitaxial region charge factor	coulomb	0.0

Model Parameters*	Description	Units	Default
RB	zero-bias (maximum) base resistance	ohm	0.0
RBM	minimum base resistance	ohm	**RB**
RC	collector ohmic resistance	ohm	0.0
RCO ‡	epitaxial region resistance	ohm	0.0
RE	emitter ohmic resistance	ohm	0.0
TF	ideal forward transit time	sec	0.0
TR	ideal reverse transit time	sec	0.0
TRB1	RB temperature coefficient (linear)	$°C^{-1}$	0.0
TRB2	RB temperature coefficient (quadratic)	$°C^{-2}$	0.0
TRC1	RC temperature coefficient (linear)	$°C^{-1}$	0.0
TRC2	RC temperature coefficient (quadratic)	$°C^{-2}$	0.0
TRE1	RE temperature coefficient (linear)	$°C^{-1}$	0.0
TRE2	RE temperature coefficient (quadratic)	$°C^{-2}$	0.0
TRM1	RBM temperature coefficient (linear)	$°C^{-1}$	0.0
TRM2	RBM temperature coefficient (quadratic)	$°C^{-2}$	0.0
T_ABS	absolute temperature	°C	
T_MEASURED	measured temperature	°C	
T_REL_GLOBAL	relative to current temperature	°C	
T_REL_LOCAL	relative to AKO model temperature	°C	
VAF (VA)	forward Early voltage	volt	infinite
VAR (VB)	reverse Early voltage	volt	infinite
VJC (PC)	base-collector built-in potential	volt	0.75
VJE (PE)	base-emitter built-in potential	volt	0.75
VJS (PS)	substrate p-n built-in potential	volt	0.75
VO	carrier mobility knee voltage	volt	10.0
VTF	transit time dependency on Vbc	volt	infinite
XCJC	fraction of **CJC** connected internally to Rb		1.0
XCJC2	fraction of **CJC** connected internally to Rb		1.0
XTB	forward and reverse beta temperature coefficient		0.0
XTF	transit time bias dependence coefficient		0.0
XTI (PT)	IS temperature effect exponent		3.0

* For information on **T_MEASURED**, **T_ABS**, **T_REL_GLOBAL**, and **T_REL_LOCAL**, see **.MODEL (Model)**.

† The parameters **ISE** (**C2**) and **ISC** (**C4**) can be set to be greater than one. In this case, they are interpreted as multipliers of **IS** instead of absolute currents: that is, if **ISE** is greater than one, then it is replaced by **ISE**·**IS**. Likewise for **ISC**.

‡ If the model parameter **RCO** is specified, then quasi-saturation effects are included.

Distribution of the CJC capacitance

The distribution of the CJC capacitance is specified by **XCJC** and **XCJC2**. The model parameter **XCJC2** is used like **XCJC**. The differences between the two parameters are as follows.

Branch	XCJC	XCJC2
intrinsic base to intrinsic collector	**XCJC*CJC**	**XCJC2*CJC**
extrinsic base to **intrinsic** collector	**(1.0 – XCJC)*CJC**	not applicable
extrinsic base to **extrinsic** collector	not applicable	**(1.0 – XCJC2)*CJC**

When **XCJC2** is specified in the range `0 <` **XCJC2** `< 1.0`, **XCJC** is ignored. Also, the extrinsic base to extrinsic collector capacitance (Cbx2) and the gain-bandwidth product (Ft2) are included in the operating point information (in the output listing generated during a Bias Point Detail analysis, **.OP (Bias Point)**). For backward compatibility, the parameter **XCJC** and the associated calculation of Cbx and Ft remain unchanged. Cbx and Ft appears in the output listing only when **XCJC** is specified.

The use of **XCJC2** produces more accurate results because Cbx2 (the fraction of **CJC** associated with the intrinsic collector node) now equals the ratio of the device's emitter area-to-base area. This results in a better correlation between the measured data and the gain bandwidth product (Ft2) calculated by PSpice.

Bipolar Transistor Equations

The equations in this section describe an NPN transistor. For the PNP and LPNP devices, reverse the signs of all voltages and currents.

The following variables are used:

Vbe = intrinsic base-intrinsic emitter voltage

Vbc = intrinsic base-intrinsic collector voltage

Vbs = intrinsic base-substrate voltage

Vbw = intrinsic base-extrinsic collector voltage (quasi-saturation only)

Vbx = extrinsic base-intrinsic collector voltage

Vce = intrinsic collector-intrinsic emitter voltage

Vjs = (NPN) intrinsic collector-substrate voltage
= (PNP) intrinsic substrate-collector voltage
= (LPNP) intrinsic base-substrate voltage

Vt = $k \cdot T/q$ (thermal voltage)

k = Boltzmann's constant

q = electron charge

T = analysis temperature (°K)

Tnom = nominal temperature (set using the TNOM option)

Other variables are listed in **Bipolar Transistor Model Parameters**.

Positive current is current flowing into a terminal.

Bipolar Transistor Equations for DC Current

Ib = base current = *area*·(Ibe1/**BF** + Ibe2 + Ibc1/**BR** + Ibc2)

Ic = collector current = *area*·(Ibe1/Kqb - Ibc1/Kqb - Ibc1/**BR** - Ibc2)

Ibe1 = forward diffusion current = **IS**·($e^{Vbe/(NF \cdot Vt)}$-1)

Ibe2 = non-ideal base-emitter current = **ISE**·($e^{Vbe/(NE \cdot Vt)}$-1)

Ibc1 = reverse diffusion current = **IS**·($e^{Vbc/(NR \cdot Vt)}$-1)

Ibc2 = non-ideal base-collector current = **ISC**·($e^{Vbc/(NC \cdot Vt)}$-1)

Kqb = base charge factor = Kq1·(1+(1+4·Kq2)^{NK})/2

Kq1 = 1/(1 - Vbc/**VAF** - Vbe/**VAR**)

Kq2 = Ibe1/**IKF** + Ibc1/**IKR**

Is = substrate current = *area*·**ISS**·($e^{Vjs/(NS \cdot Vt)}$-1)

Rb = actual base parasitic resistance

Case 1

for: **IRB** = infinite (default value)

then: Rb = (**RBM** + (**RB**-**RBM**)/Kqb)/*area*

Case 2

For: **IRB** > 0

then:
Rb = (**RBM** + 3·(**RB**-**RBM**)· $\frac{\tan(x) - x}{x \cdot (\tan(x))^2}$)/*area*

where:
$x = \frac{(1 + (144/\pi^2) \cdot Ib/(area \cdot \mathbf{IRB}))^{1/2} - 1}{(24/\pi^2) \cdot (Ib/(area \cdot \mathbf{IRB}))^{1/2}}$

Bipolar Transistor Equations for Capacitance

All capacitances, except Cbx, are between terminals of the intrinsic transistor which is inside of the collector, base, and emitter parasitic resistances. Cbx is between the intrinsic collector and the extrinsic base.

Base-Emitter Capacitance

Cbe = base-emitter capacitance = Ctbe + *area*·Cjbe

Ctbe = transit time capacitance = tf·Gbe

tf = effective **TF** = **TF**·(1+**XTF**·(Ibe1/(Ibe1+*area*·**ITF**))^2·$e^{Vbc/(1.44\cdot VTF)}$)

Gbe = DC base-emitter conductance = (*d*Ibe)/(*d*Vb)

Ibe = Ibe1 + Ibe2

Cjbe = **CJE**·(1-Vbe/**VJE**)$^{-MJE}$ *IF* Vbe ≤ **FC**·**VJE**

Cjbe = **CJE**·(1-**FC**)$^{-(1+MJE)}$·(1-**FC**·(1+**MJE**) +**MJE**·Vbe/**VJE**) *IF* Vbe > **FC**·**VJE**

Base-Collector Capacitance

Cbc = base-collector capacitance = Ctbc + *area*·**XCJC**·Cjbc

Ctbc = transit time capacitance = **TR**·Gbc

Gbc = DC base-collector conductance = (*d*Ibc)/(*d*Vbc)

Cjbc = **CJC**·(1-Vbc/**VJC**)$^{-MJC}$ *IF* Vbc < **FC**·**VJC**

Cjbc = **CJC**·(1-**FC**)$^{-(1+MJC)}$·(1 **FC**·(1+**MJC**)+**MJC**·Vbc/**VJC**) *IF* Vbc > **FC**·**VJC**

Extrinsic-Base to Intrinsic-Collector Capacitance

Cbx = extrinsic-base to intrinsic-collector capacitance = *area*·(1-**XCJC**)·Cjbx

Cjbx = **CJC**·(1-Vbx/**VJC**)$^{-MJC}$ *IF* Vbx ≤ **FC**·**VJC**

Cjbx = **CJC**·(1-**FC**)$^{-(1+MJC)}$·(1-**FC**·(1+**MJC**)+**MJC**·Vbx/**VJC**) *IF* Vbx > **FC**·**VJC**

Substrate Junction Capacitance

Cjs = substrate junction capacitance = *area*·Cjjs

Cjjs = **CJS**·(1-Vjs/**VJS**)$^{-MJS}$(assumes **FC** = 0) *IF* Vjs ≤ 0

Cjjs = **CJS**·(1+**MJS**·Vjs/**VJS**) *IF* Vjs > 0

Bipolar Transistor Equations for Quasi-Saturation Effect

Quasi-saturation is an operating region where the internal base-collector metallurgical junction is forward biased, while the external base-collector terminal remains reverse biased.

This effect is modeled by extending the intrinsic Gummel-Poon model, adding a new internal node, a controlled current source, Iepi, and two controlled capacitances, represented by the charges Qo and Qw. These additions are only included if the model parameter **RCO** is specified. See reference [3] of **References** for the derivation of this extension.

Iepi = *area*·(**VO**·(Vt·(K(Vbc)-K(Vbn)-*ln*((1+K(Vbc))/(1+K(Vbn))))+Vbc-Vbn))/**RCO**·(|Vbc-Vbn|+**VO**)

Qo = *area*·**QCO**·(K(Vbc)-1-**GAMMA**/2)

Qw = *area*·**QCO**·(K(Vbn)-1-**GAMMA**/2)

where

$K(v) = (1+\mathbf{GAMMA}\cdot e^{(v/Vt)})^{1/2}$

Bipolar Transistor Equations for Temperature Effect

IS(T) = **IS**·$e^{(T/Tnom-1)\cdot EG/(N\cdot Vt)}$·$(T/Tnom)^{XTI/N}$
where N = 1

ISE(T) = (**ISE**/$(T/Tnom)^{XTB}$)·$e^{(T/Tnom-1)\cdot EG/(NE\cdot Vt)}$·$(T/Tnom)^{XTI/NE}$

ISC(T) = (**ISC**/$(T/Tnom)^{XTB}$)·$e^{(T/Tnom-1)\cdot EG/(NC\cdot Vt)}$·$(T/Tnom)^{XTI/NC}$

ISS(T) = (**ISS**/$(T/Tnom)^{XTB}$)·$e^{(T/Tnom-1)\cdot EG/(NS\cdot Vt)}$·$(T/Tnom)^{XTI/NS}$

BF(T) = **BF**·$(T/Tnom)^{XTB}$

BR(T) = **BR**·$(T/Tnom)^{XTB}$

RE(T) = **RE**·(1+**TRE1**·(T-Tnom)+**TRE2**·$(T-Tnom)^2$)

RB(T) = **RB**·(1+**TRB1**·(T-Tnom)+**TRB2**·$(T-Tnom)^2$)

RBM(T) = **RBM**·(1+**TRM1**·(T-Tnom)+**TRM2**·$(T-Tnom)^2$)

RC(T) = **RC**·(1+**TRC1**·(T-Tnom)+**TRC2**·$(T-Tnom)^2$)

VJE(T) = **VJE**·T/Tnom - 3·Vt·*ln*(T/Tnom) - Eg(Tnom)·T/Tnom + Eg(T)

VJC(T) = **VJC**·T/Tnom - 3·Vt·*ln*(T/Tnom) - Eg(Tnom)·T/Tnom + Eg(T)

VJS(T) = **VJS**·T/Tnom - 3·Vt·*ln*(T/Tnom) - Eg(Tnom)·T/Tnom + Eg(T)

where Eg(T) = silicon bandgap energy = 1.16 - .000702·T^2/(T+1108)

CJE(T) = **CJE**·(1+**MJE**·(.0004·(T-Tnom)+(1-**VJE**(T)/**VJE**)))

CJC(T) = **CJC**·(1+**MJC**·(.0004·(T-Tnom)+(1-**VJC**(T)/**VJC**)))

CJS(T) = **CJS**·(1+**MJS**·(.0004·(T-Tnom)+(1-**VJS**(T)/**VJS**)))

Bipolar Transistor Equations for Noise

Noise is calculated assuming a 1.0-hertz bandwidth, using the following spectral power densities (per unit bandwidth):

Parasitic Resistances Thermal Noise	
RC	$Ic^2 = 4 \cdot k \cdot T/(RC/area)$
RB	$Ib^2 = 4 \cdot k \cdot T/RB$
RE	$Ie^2 = 4 \cdot k \cdot T/(RE/area)$
Base and Collector Currents Shot and Flicker Noise	
IB	$Ib^2 = 2 \cdot q \cdot Ib + KF \cdot Ib^{AF}/FREQUENCY$
IC	$Ic^2 = 2 \cdot q \cdot Ic$

References

For a more information on bipolar transistor models, refer to:

[1] Ian Getreu, Modeling the Bipolar Transistor, Tektronix, Inc. part# 062-2841-00.

For a generally detailed discussion of the U.C. Berkeley SPICE models, including the bipolar transistor, refer to:

[2] P. Antognetti and G. Massobrio, Semiconductor Device Modeling with SPICE, McGraw-Hill, 1988.

For a description of the extension for the quasi-saturation effect, refer to:

[3] G. M. Kull, L. W. Nagel, S. W. Lee, P. Lloyd, E. J. Prendergast, and H. K. Dirks, “A Unified Circuit Model for Bipolar Transistors Including Quasi-Saturation Effects,” IEEE Transactions on Electron Devices, ED-32, 1103-1113 (1985).

Resistor

General Form

```
R<name> <(+) node> <(-) node> [model name] <value>
+ [TC = <TC1> [,<TC2>]]
```

Examples

```
RLOAD 15 0 2K
R2 1 2 2.4E4 TC=.015,-.003
RFDBCK 3 33 RMOD 10K
```

Model Form

```
.MODEL <model name> RES [model parameters]
```

Arguments and Options

(+) and (-) nodes
Define the polarity when the resistor has a positive voltage across it.

[model name]
Affects the resistance value; see **Resistor Value Formulas**.

Comments

The first node listed (or pin 1 in Schematics) is defined as positive. The voltage across the component is therefore defined as the first node voltage minus the second node voltage.

Positive current flows from the (+) node through the resistor to the (-) node. Current flow from the first node through the component to the second node is considered positive.

Temperature coefficients for the resistor can be specified in-line, as in the second example. If the resistor has a model specified, then the coefficients from the model are used for the temperature updates; otherwise, the in-line values are used. In both cases the temperature coefficients have default values of zero. Expressions cannot be used for the in-line coefficients.

Schematics Symbols

For standard R parts, the effective value of the part is set directly by the VALUE attribute. For the variable resistor, R_VAR, the effective value is the product of the base value (VALUE) and multiplier (SET).

In general, resistors should have positive component values (VALUE attribute). In all cases, components must not be given a value of zero.

However, there are cases when negative component values are desired. This occurs most often in filter designs that analyze an RLC circuit equivalent to a real circuit. When transforming from the real to the RLC equivalent, it is possible to end up with negative component values.

Chapter

PSpice A/D allows negative component values for bias point, DC sweep, AC, and noise analyses. In the case of resistors, the noise contribution from negative component values come from the absolute value of the component (components are not allowed to generate negative noise). A transient analysis may fail for a circuit with negative components. Negative components may create instabilities in time that the analysis cannot handle.

Symbol Name	Model Type	Attribute	Attribute Description
R	resistor	VALUE	resistance
		TC	linear and quadratic temperature coefficients
		TOLERANCE	device tolerance (see page 1-24)
R_VAR	variable resistor	VALUE	base resistance
		SET	multiplier

The RBREAK part must be used if you want a LOT tolerance. In that case, use the Model Editor to edit the RBREAK instance.

Breakout Parts

For non-stock passive and semiconductor devices, Schematics has a set of breakout parts designed for customizing model parameters for simulation. These are useful for setting up Monte Carlo and worst-case analyses with device and/or lot tolerances specified for individual model parameters.

Basic breakout part names consist of the intrinsic PSpice A/D device letter plus the suffix BREAK. By default, the model name is the same as the part name and references the appropriate device model with all parameters set at their default. For instance, the DBREAK part references the DBREAK model, which is derived from the intrinsic PSpice A/D D model (.MODEL DBREAK D). Another approach is to use the model editor to derive an instance model and customize this. For example, you could add device and/or lot tolerances to model parameters.

For breakout part RBREAK, the effective value is computed from a formula that is a function of the specified VALUE attribute.

Part Type	Symbol Name	Symbol Library File	Attribute	Description
resistor	RBREAK	`breakout.slb`	VALUE	resistance
			MODEL	RES model name

Resistor Model Parameters

Model Parameters*	Description	Units	Default
R	resistance multiplier		1.0
TC1	linear temperature coefficient	$°C^{-1}$	0.0
TC2	quadratic temperature coefficient	$°C^{-2}$	0.0
TCE	exponential temperature coefficient	%/°C	0.0
T_ABS	absolute temperature	°C	
T_MEASURED	measured temperature	°C	
T_REL_GLOBAL	relative to current temperature	°C	
T_REL_LOCAL	relative to AKO model temperature	°C	

* For information on **T_MEASURED**, **T_ABS**, **T_REL_GLOBAL**, and **T_REL_LOCAL**, see **.MODEL (Model)**.

Resistor Equations

Resistor Value Formulas

One

If [model name] is included and **TCE** is specified, then the resistance is given by:

$<value> \cdot R \cdot 1.01^{TCE \cdot (T-Tnom)}$

where <value> is normally positive (though it can be negative, but not zero). Tnom is the nominal temperature (set using TNOM option).

Two

If [model name] is included and **TCE** is **not** specified, then the resistance is given by:

$<value> \cdot R \cdot (1+TC1 \cdot (T-Tnom)+TC2 \cdot (T-Tnom)^2)$

where <value> is usually positive (though it can be negative, but not zero).

Resistor Equation for Noise

Noise is calculated assuming a 1.0-hertz bandwidth. The resistor generates thermal noise using the following spectral power density (per unit bandwidth):

$i^2 =$
$4 \cdot k \cdot T/resistance$