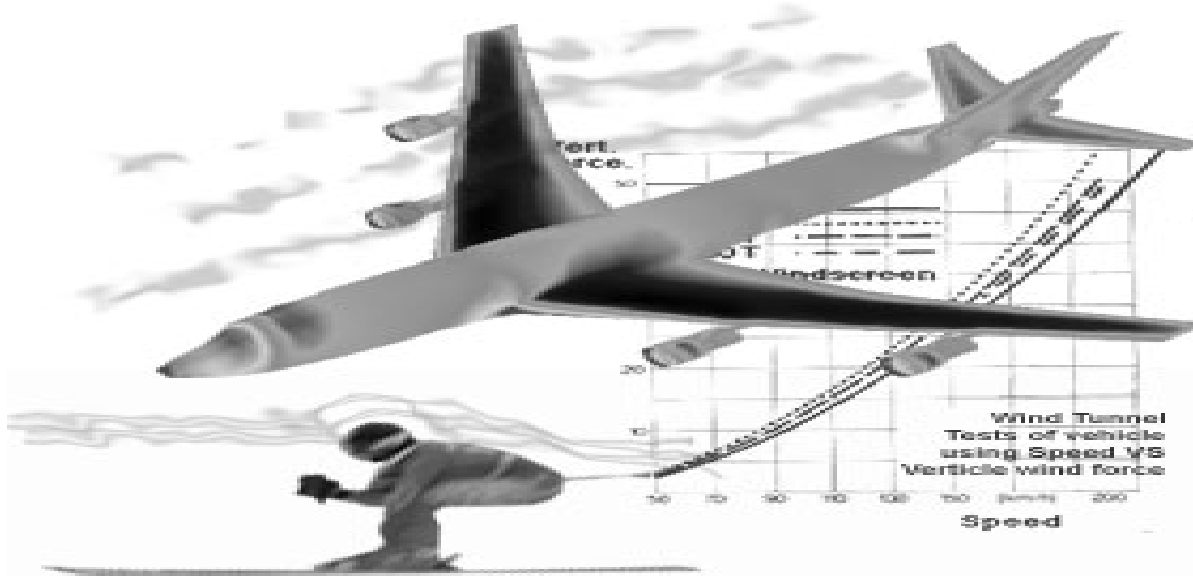




# Wide Area Distributed Pressure Sensors

**Bologna, May 24<sup>th</sup> 2002**

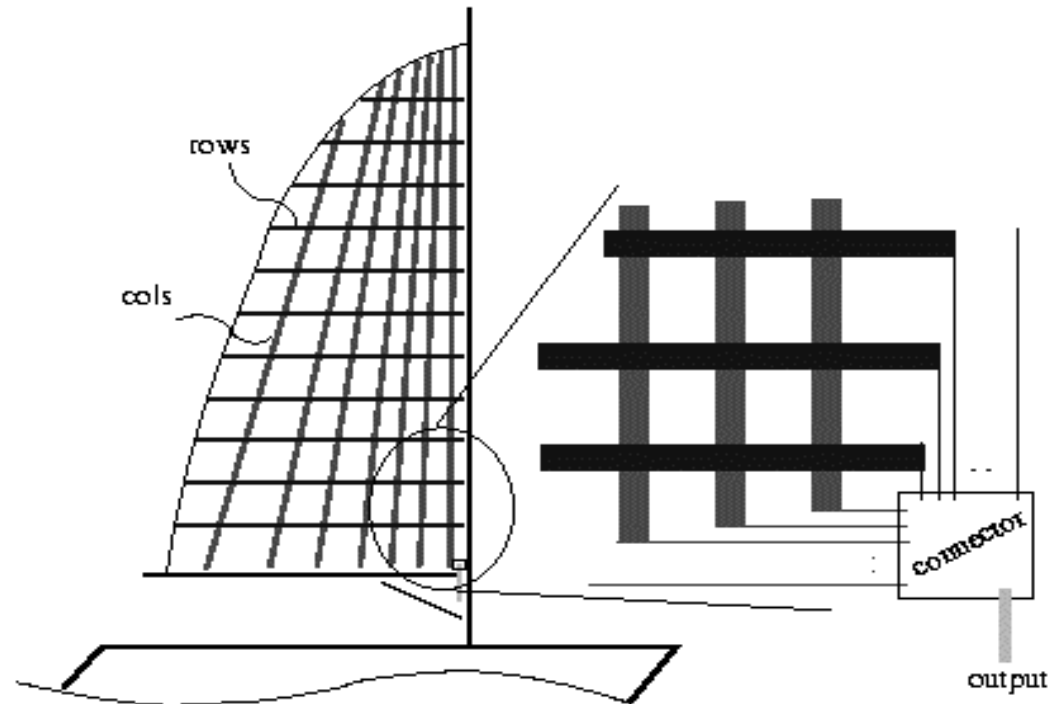
# Wide-Area Distributed Pressure Sensors



- Array of smart sensors for real-time monitoring of very large-area extended pressure fields



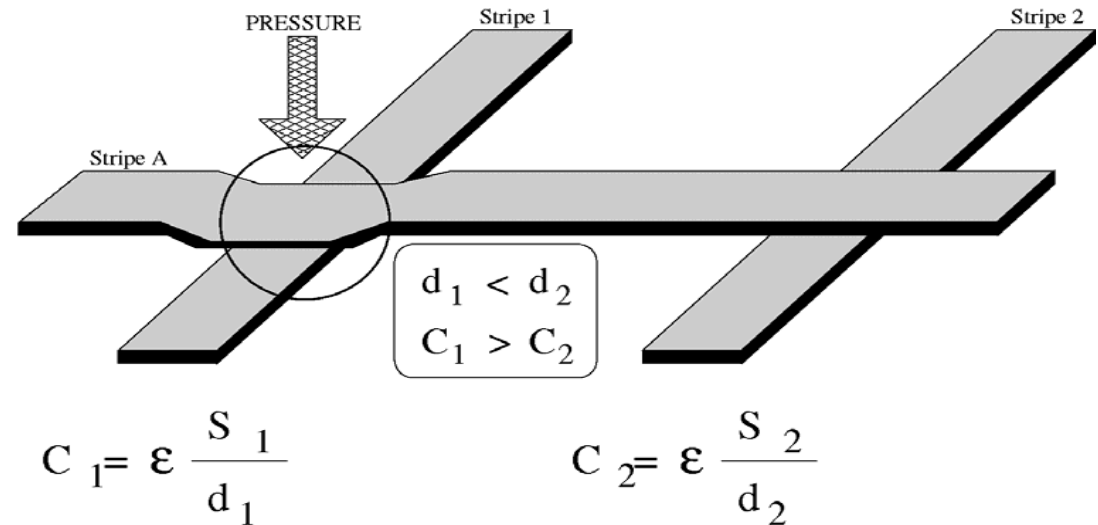
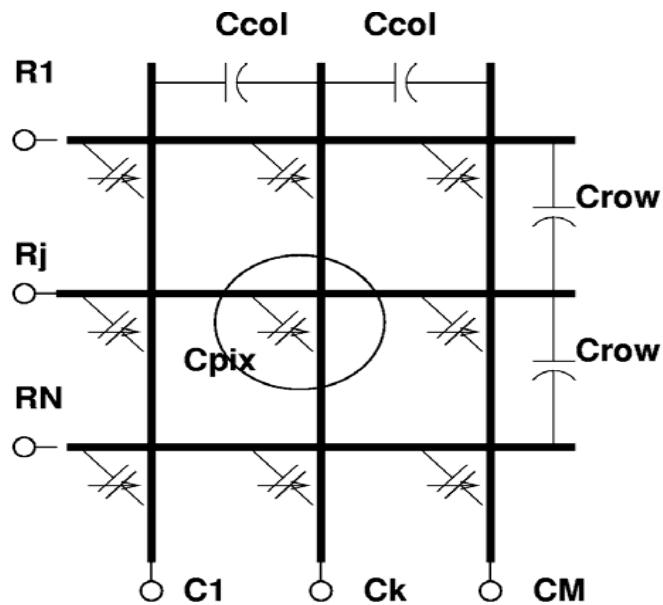
# Possible Application: E-Sail Project



- Array of Capacitive Pressure Sensitive Sensors
- Sail Trimming for Best Performance



# BASIC IDEA



- Distributed array of passive sensing elements
  - Conductive threads separated by an elastic insulator
- Capacitive sensing
  - Charge/voltage conversion



# SYSTEM LEVEL ISSUES

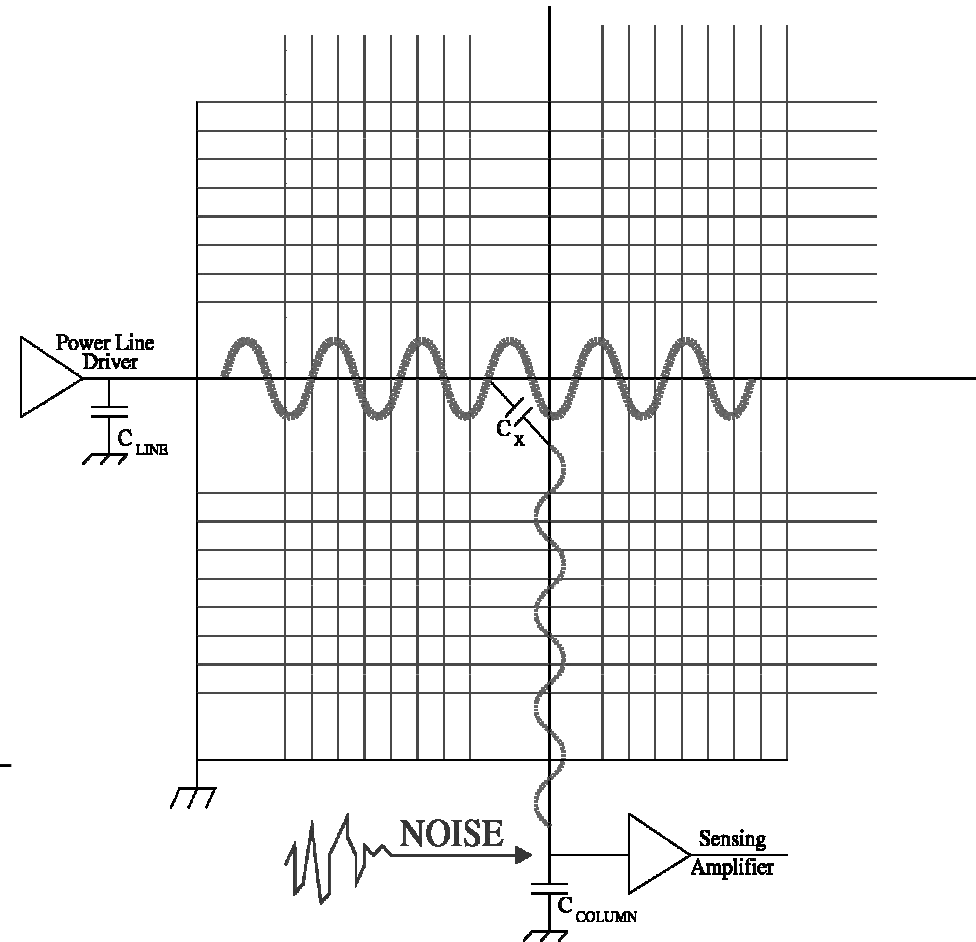
- Parasitic capacitances
  - 1-3 order of magnitude greater than sensed cap.
- Long distance
  - Transmission lines
  - Electromagnetic interferences
- Unobtrusiveness
  - Reduced number of I/O



# FAR & SMALL CAPACITANCE

## MEASURE

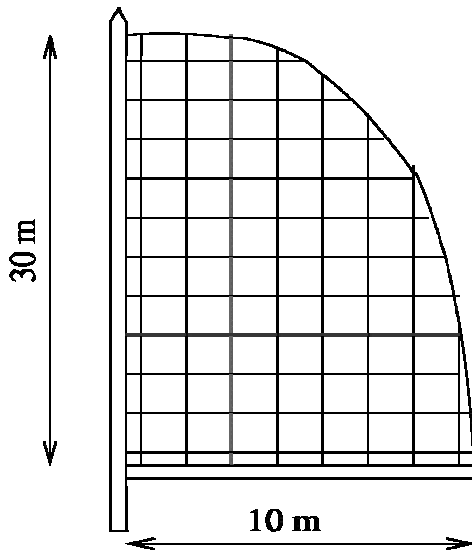
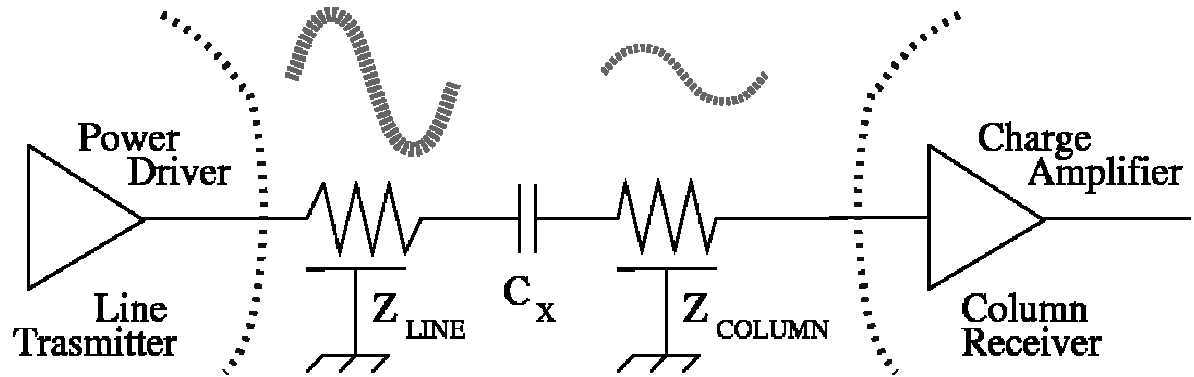
- Sensing strategies:
  - Sine function through  $C_X$
  - Unselected lines grounded
- Sensing problems:
  - Heavy  $C_{ROW}$  driving
  - Long line propagation & R-C effects
  - Precise evaluation of  $C_X \ll C_{COL}$
  - Crosstalk and noise effects



# SIGNAL PATH MODEL

## Simplified model:

- Wave Stationary
- Negligible L effects

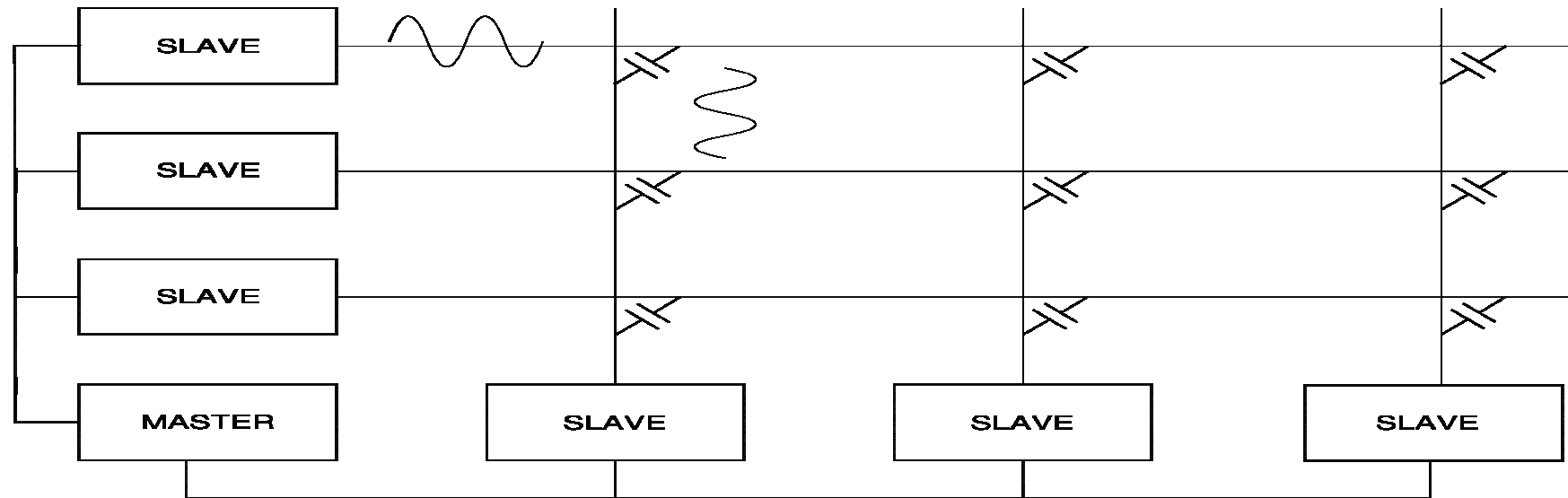


## Target application: E-SAIL

- Line length 10-30 m
  - quasi static conditions if freq. < 10 MHz
- Aluminium thin & large strips
  - R very small, C meanly concentrated



# PROPOSED ARCHITECTURE

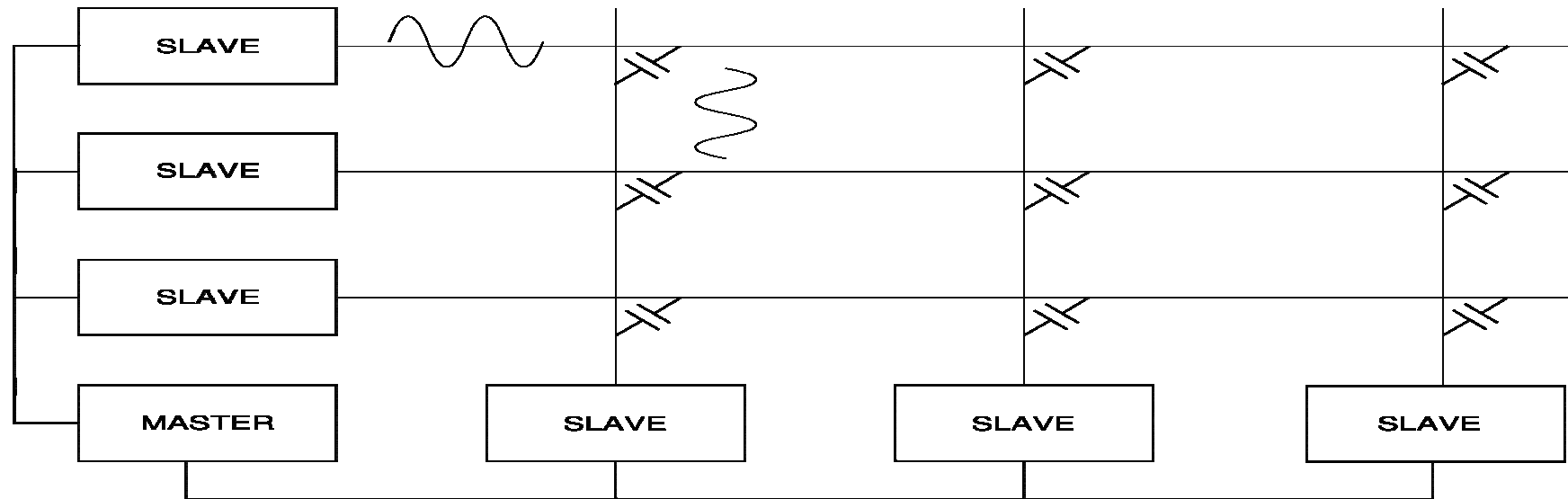


- Distributed addressing and sensing
  - Row modules: stimulus generation
  - Column modules: read-out & data processing
  - Digital bus: synchronization and data transfer





# PROPOSED ARCHITECTURE



- Row-wise array scanning
- Master/Slave communication
- Autonomous modules based distributed computation

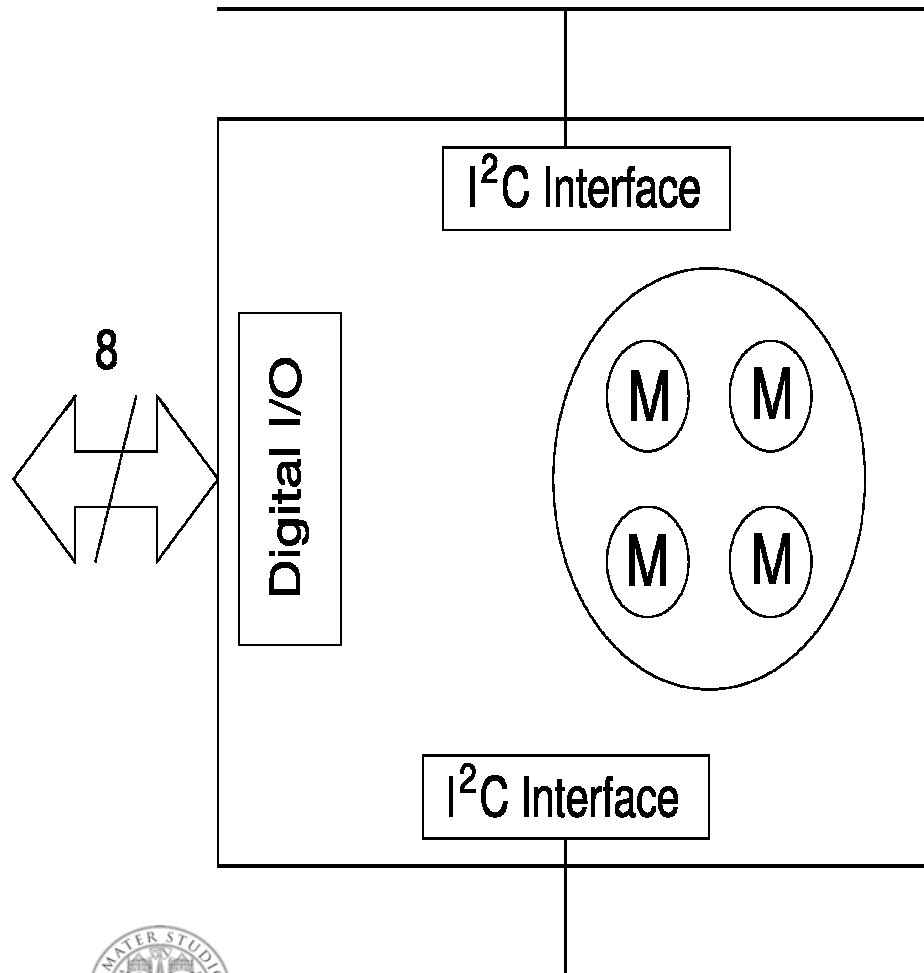


# COMMUNICATION: BUS MODULE

- I<sup>2</sup>C-based 2-wire digital bus split in 2 different modules
  - Vertical bus: used to address each row block  
(Single direction communication, addressed mode)
  - Horizontal bus: used to collect data  
(Single direction communication, fast mode)
- Horizontal & Vertical bus: System bootstrap  
(Broadcast communication)



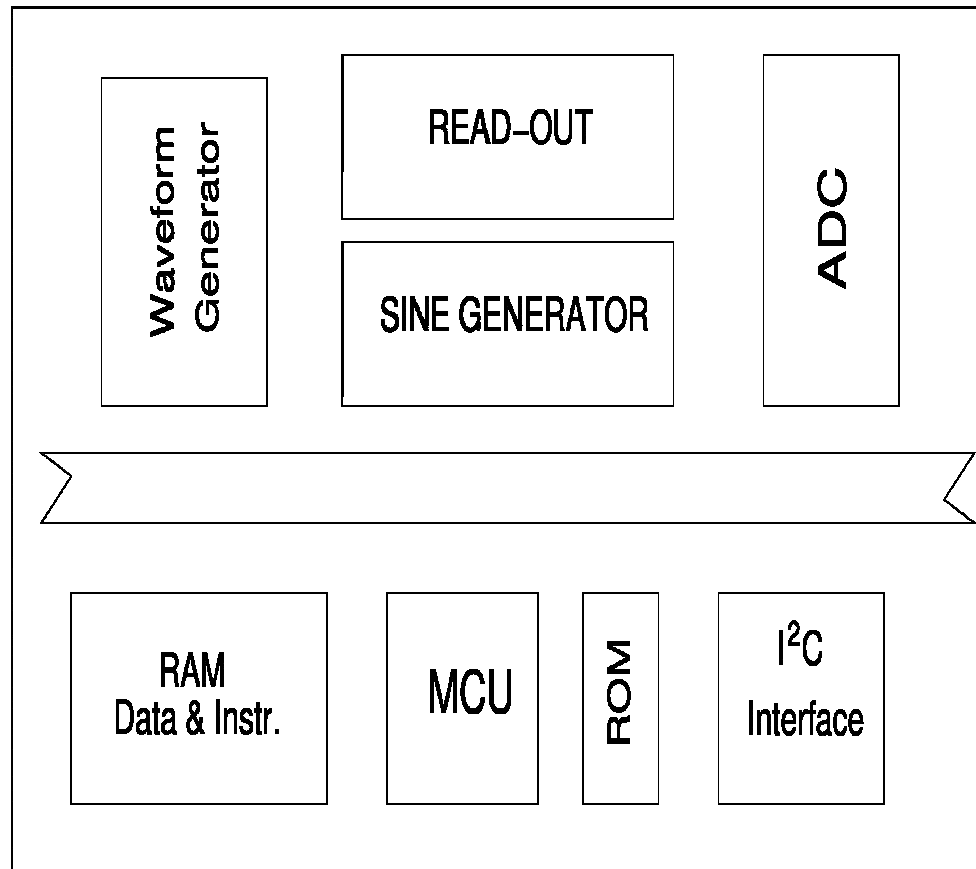
# MASTER MODULE



- Cluster of communication masters with static priority
- Two I<sup>2</sup>C master interfaces
  - Internal data transfer
- 8-bit digital interface
  - External communication
- Microcontroller
  - Data elaboration
  - Protocol synchronization



# SLAVE MODULE

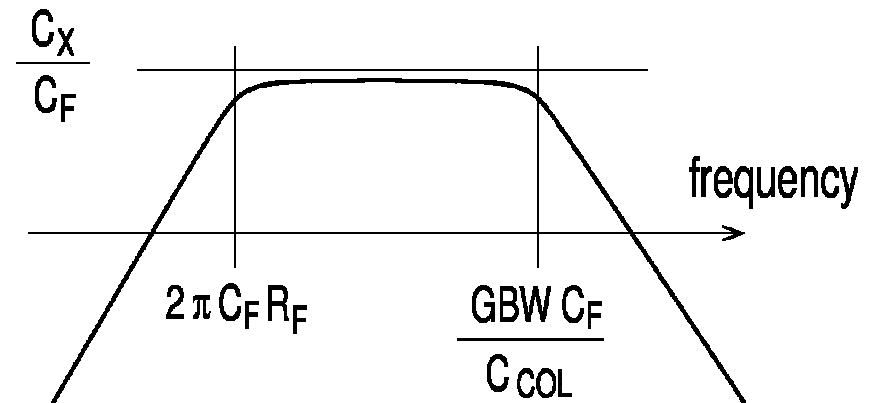
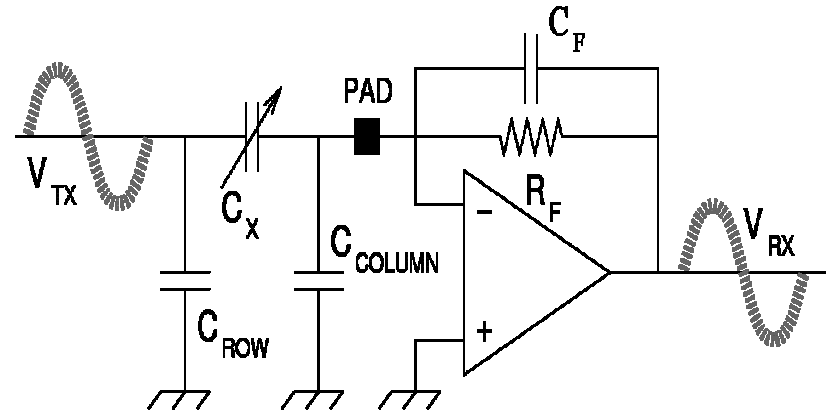


- Reduced pin number:
  - 3 I/O (2 digital, 1 analog)
  - 2 power supply
- Analog core:
  - Sine wave generation
  - Sense – Filtering
  - Addressing
- Digital core:
  - Early data processing
  - Data transfer
  - Synchronization protocol

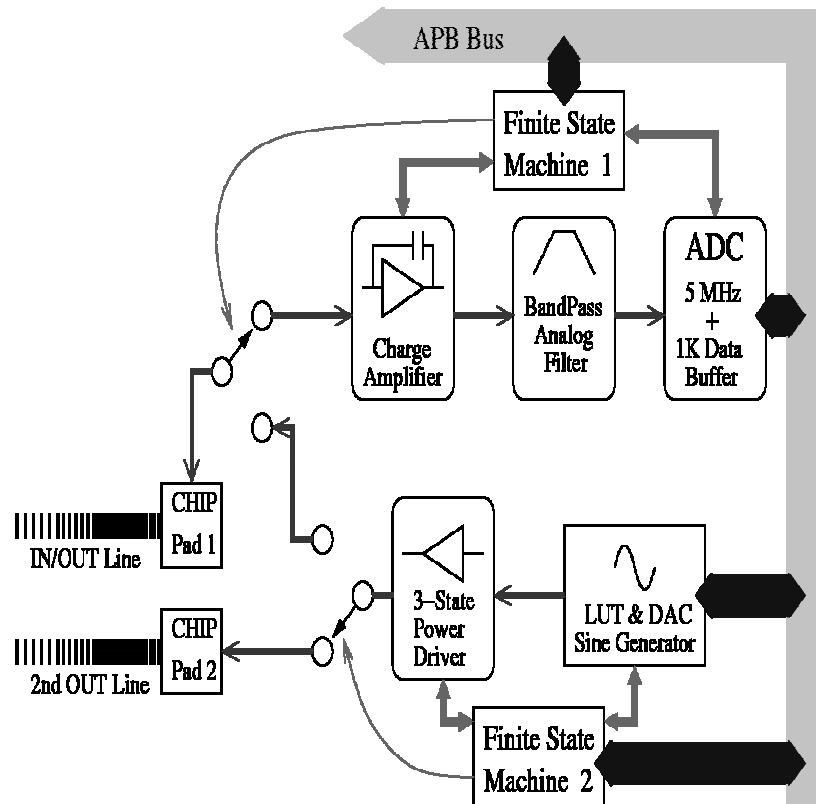


# AC CHARGE AMPLIFIER

- $C_F$  calculation  
( $V_{TX}$  and  $V_{RX}$  full range)
- Op. Amp.  $A_0 \gg 1$   
( $C_{COLUMN}$  negligible)
- $f_0$  centered
- Further  $V_{RX}$  filtering



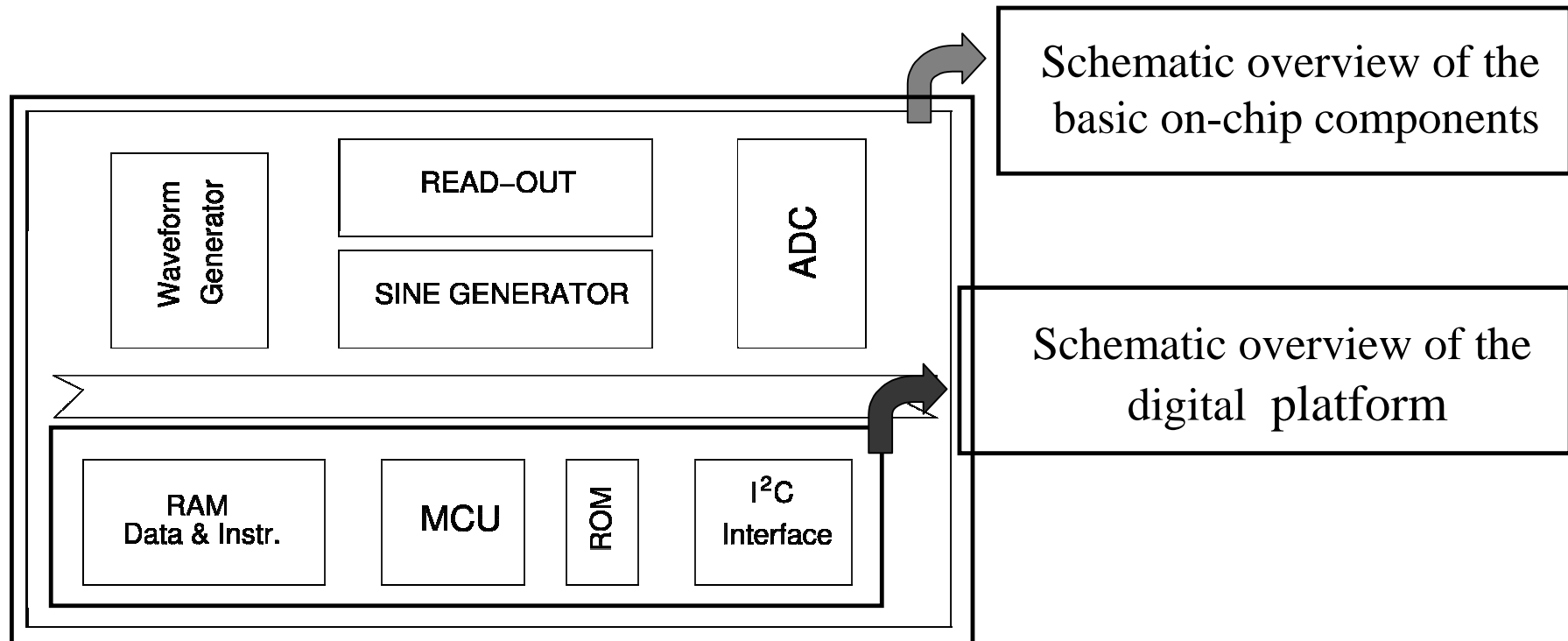
# ANALOG CORE OVERVIEW



- Sine generation module:
  - Digital counter
  - Programmable lookup table
  - DA converter
- Signal driver & receiver:
  - Same chip for rows and columns
  - Stand alone sensor achievable



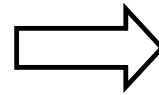
# Digital platform for smart sensor



# Basic Components for smart sensor

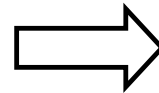
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Embedded elaboration unit



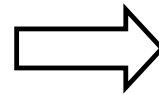
16-bit XiRisc processor

Two-wire interface (40m, 1Mbps)



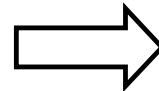
I<sup>2</sup>C Controller

Control of analog components  
(stimuli generation, A/D conversion)



On-chip dedicated FSMs

Boot load



Dedicated FSM inside the I<sup>2</sup>C Unit



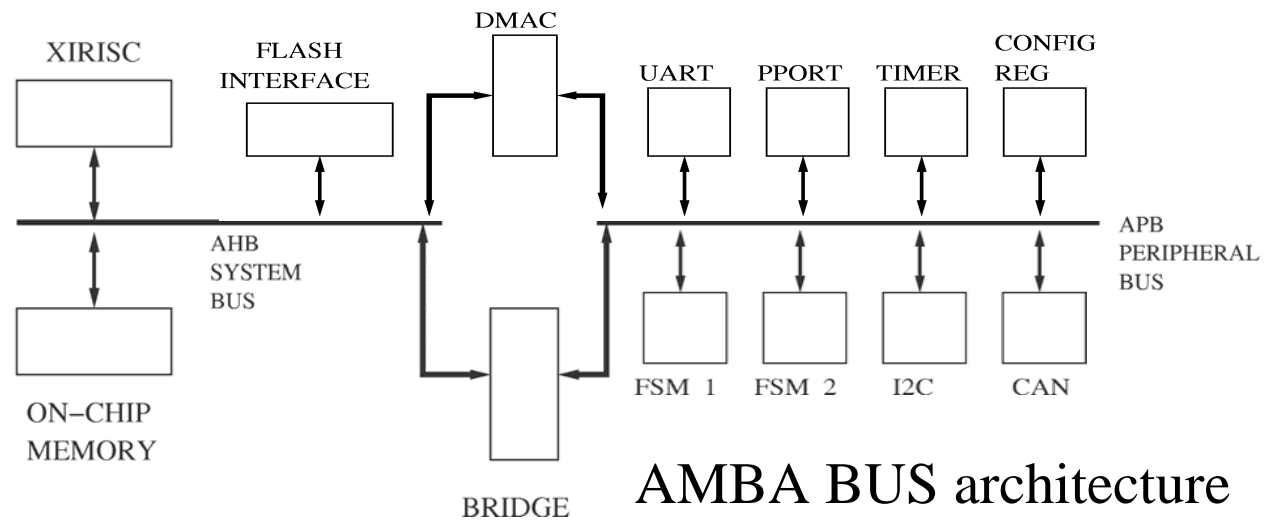


# System-on-Chip Scenario

## (easy-to-plug in peripherals)

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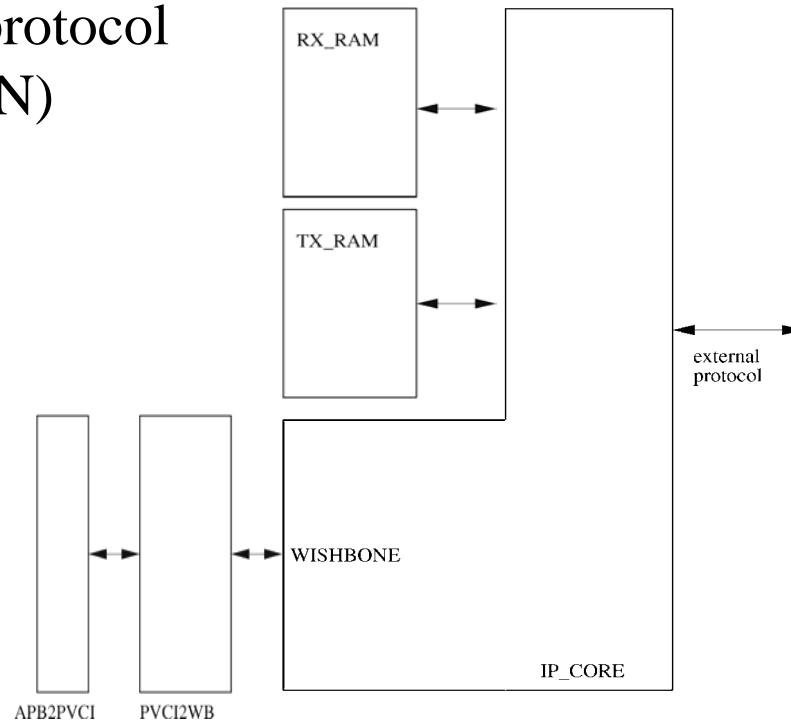
- (red boxes) basic components for a smart-sensor environment
- (black boxes) additional available general-purpose components



# IP CORE Structural Overview

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- IP (Open Source) + external protocol (RS232, IEEE 1284, I<sup>2</sup>C, CAN)
- VSIA standard interface
- APB AMBA wrapper
- RAM Fifo Buffer



# SILICON INTEGRATION

- Digital Front to Back Design flow for HCMOS8
- Tape out: 3Q 2002
- Analog Core:
  - Reuse of hard blocks and custom layout
- Digital Core:
  - Soft macro internal library



# PROJECT STATUS AND FUTURE DIRECTIONS

- Smart textile: Haptic interface
  - Gesture recognition: biometric identification
  - Biomedical devices: smart body cast
  - 3 papers accepted, 1 paper submitted, 2 patents pending
- Ultra wide area pressure sensors
  - Aerodynamic: real time pressure profile
  - 1 paper accepted, 1 patent pending

