Trends and Challenges in VLSI Technology Scaling Towards 100nm

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Agenda

• **VLSI Technology Trends**
  – Frequency and power trends

• **Scaling Challenges**
  – Transistor scaling
  – Interconnect scaling
  – Capacitive and inductive coupling
  – Leakage

• **Summary**
Process Technology Evolution

1961
First Planar Integrated Circuit
Two transistors

2001
Pentium® 4 Processor
42 million transistors
Moore’s Law - 1965

Cramming more components onto integrated circuits

With unit cost falling as the number of components per circuit rises, by 1975 economics may dictate squeezing as many as 5,000 components on a single silicon chip.

By Gordon E. Moore
Moore’s Law - Today

- Number of transistors per integrated circuit doubles every two years
## SIA Technology Roadmap

<table>
<thead>
<tr>
<th></th>
<th></th>
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<th></th>
</tr>
</thead>
<tbody>
<tr>
<td>Process Technology [nm]</td>
<td>180</td>
<td>130</td>
<td>90</td>
<td>60</td>
</tr>
<tr>
<td>Logic Transistors [mil]</td>
<td>23.8</td>
<td>47.6</td>
<td>135</td>
<td>539</td>
</tr>
<tr>
<td>Across-chip Clock Speed [MHz]</td>
<td>1200</td>
<td>1600</td>
<td>2000</td>
<td>2655</td>
</tr>
<tr>
<td>Die area [sq. mm]</td>
<td>340</td>
<td>340</td>
<td>390</td>
<td>468</td>
</tr>
<tr>
<td>Wiring Levels</td>
<td>6</td>
<td>7</td>
<td>8</td>
<td>9</td>
</tr>
</tbody>
</table>
ITRS Roadmap Acceleration Continues

![Graph showing feature size (nm) vs. year of production from 1994 to 2000. The graph shows a trend of decreasing feature sizes with time, indicating continuous acceleration in semiconductor production technology.]
• Frequency doubles each generation
• Number of gates per clock reduces by 25%
Bus frequency is not keeping up with the processor core
• Lead processor power increases every generation
• Compactions provide higher performance at lower power
Power Density Trend

- Assumptions: 15mm die, 1.5x frequency increase per generation
Voltage Scaling

Supply Voltage [V]

~0.7X Scaling

~0.85X Scaling

Year

1991 1993 1995 1997 1999 2001 2003 2005 2007

0.1

1

10
0.13\(\mu\)m Process Technology

70nm Lgate NMOS transistor – in production today

Source: S. Tyagi, et.al., IEDM 2000
Transistor Physical Gate Length

Year

Micron

Technology Node

Transistor Physical Gate Length

Source: Robert Chau, 6/2001
30nm Physical Gate Length Transistor

For the 65nm technology node – production 2005

Source: R. Chau, et.al., IEDM 2000
Transistor Physical Gate Length

Year

1991 1993 1995 1997 1999 2001 2003 2005 2007 2009

Micron

0.01 0.1 1

Technology Node

Transistor Physical Gate Length

Source: R. Chau, 6/2001
Research Transistor with 20nm Physical Gate Length

For the 45nm technology node – research phase

Source: R. Chau, et.al., SNW 2001
Oxide Thickness Scaling

Source: T. Ghani, VLSI Symposium, 2000

Technology Generation [um]

Oxide Thickness [nm]

T$_{ox}$ (Electrical)

Equivalent Oxide Thickness (Physical)
Atoms-Thin Gate Oxide

Source: R. Chau, et.al., IEDM 2000
Moore’s Law + 300mm Wafers = 4x advantage

• Moore’s Law:
  – From 0.18µm to 0.13µm = 2x output

• 300mm Wafers:
  – From 200mm to 300mm = 2x output

• Combined output advantage:
  – 4x output
0.13µm Production Ramp

- Six factories readying 0.13µm production
  - Plan to spend $7.5B on capital in 2001
- Yields and volume exceeding expectations
  - 0.13µm products have been shipping since May
Lithography Challenges


Micron: 0.1, 0.01

- Lithography Wavelength
- Silicon Feature Size
Extreme Ultraviolet Lithography

• EUV lithography uses extremely short wavelength light (20x shorter than today’s lithography processes)
  – *Visible light* – 400 to 700 nm
  – *DUV lithography* – 193 and 248 nm
  – *EUV lithography* – 13 nm

• Will be used first in 2005 for critical lithography steps to produce 70 nm patterns
• SRAM cell size will continue to scale ~0.5x per generation
Exploit Memory Power Efficiency

- Static memory has 10X lower active power density
- Lower leakage than logic
- Integrated L2 provides higher bandwidth and lower latency
Example: Pentium® III Processor Evolution

- 0.18μm technology
- 256KB L2
- 28 million transistors
- 106 mm² die size

- 0.13μm technology
- 512KB L2
- 44 million transistors
- 80 mm² die size
Bit Line Delay Scaling

- Bit line swing limited by parameter mismatch & differential noise
- Cell stability degrades with Vt lowering
- Reducing number of rows per bitline approaching limit
Process Fluctuations

Die-to-Die Fluctuations
- Resist Thickness

Within-Die Fluctuations
- Systematic
- Lens Aberrations
- Random
- Random Placement of Dopant Atoms

Source: K. Bowman, et.al., ISSCC’2001
0.18µm Al Interconnect

Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Transistors
Wires Are Not Scaling Well

![Graph showing the delay in nanoseconds (ps) as a function of process generation in micrometers (um). The graph compares different wire and gate configurations, including Al wires + SiO2, Cu wires + lowK, Gate + Al wires, and Gate + Cu wires. The source of the data is SIA NTRS projection.]
0.13μm Cu Interconnect

Metal 6
Metal 5
Metal 4
Metal 3
Metal 2
Metal 1
Transistors

Source: S. Tyagi, et.al., IEDM 2000
Metal Layers

Number of Metal Layers

Technology Generation [um]

<table>
<thead>
<tr>
<th>Technology Generation [um]</th>
<th>Number of Metal Layers</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.5</td>
<td>2</td>
</tr>
<tr>
<td>1</td>
<td>2</td>
</tr>
<tr>
<td>0.8</td>
<td>3</td>
</tr>
<tr>
<td>0.6</td>
<td>4</td>
</tr>
<tr>
<td>0.35</td>
<td>5</td>
</tr>
<tr>
<td>0.25</td>
<td>5.5</td>
</tr>
<tr>
<td>0.18</td>
<td>6.3</td>
</tr>
<tr>
<td>0.13</td>
<td>6.5</td>
</tr>
</tbody>
</table>
Metal Aspect Ratios

Average Aspect Ratio

Technology Generation [um]

- 1.5  1.0  0.8  0.6  0.35  0.25  0.18  0.13
Interconnect RC Delay vs. Pitch

- 40% lower RC delay by using Cu + FSG ILD

Source: S. Tyagi, et.al., IEDM 2000
<table>
<thead>
<tr>
<th>Layer</th>
<th>Routing Type</th>
<th>Metal Layers</th>
<th>Description</th>
</tr>
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<tbody>
<tr>
<td>M1</td>
<td>Local Wiring</td>
<td>3</td>
<td>Block-level routing</td>
</tr>
<tr>
<td>M2</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M3</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M4</td>
<td>Semi-Global Wiring</td>
<td>2</td>
<td>Unit-level routing</td>
</tr>
<tr>
<td>M5</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>M6</td>
<td>Fat Wiring</td>
<td>2</td>
<td>Cluster-level routing</td>
</tr>
<tr>
<td>M7</td>
<td></td>
<td></td>
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<tr>
<td>M8</td>
<td>Super-Fat Wiring</td>
<td>Top 2 layers</td>
<td>Global routing</td>
</tr>
<tr>
<td>M9</td>
<td></td>
<td></td>
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</tr>
</tbody>
</table>
Noise Sources

- **Capacitive Coupling**
  - Due to electric field
  - “Near” field effect
  - Measures resistance to a voltage change

- **Inductive Coupling**
  - Due to magnetic field
  - “Far” field effect
  - Measures resistance to a current change
  - Frequency dependent
Inductive Noise

- Inductance of VLSI metal lines is becoming important at operating frequencies above 1GHz

PCB (FR4) Signal Trace

VLSI Metal Line
Effects of Capacitive Coupling

- Capacitive coupling can translate into a noise problem

- or a delay problem

![Diagram showing effects of capacitive coupling between aggressor and victim circuits](image-url)
Worst Case Input Patterns

- C-only
- L-only
- C & L cancel
- C & L additive

- Near attackers couple mostly by capacitance
- Far attackers couple mostly by inductance
- Lenz’s law - a change in current will generate an opposing current which resists the change
- Worst-case switching pattern when near and far attackers switch anti-phase
Inductive Noise Impact on Delay

- Capacitive noise effect on delay is modeled by coupling coefficient.
- Inductive noise affects delay too.
- Inductive noise can also decrease delay.

Graph showing RLC delay with far-attackers switching up and down, compared to RC only delay.
Skin Effect in VLSI Circuits

- Edge frequency is 5-9x the clock frequency
Sub-Threshold Leakage

- Sub-threshold leakage increases for lower channel lengths and lower $V_T$'s
Estimated Power of a 15mm Processor

- **0.25µm, 2V**
  - Power (Watts)
  - Leakage: 0% 0% 0% 0% 1% 1% 1% 2% 3%
  - Active: 0% 0% 0% 0% 0% 0% 0% 0% 0%
  - Temp (C): 30 40 50 60 70 80 90 100 110

- **0.18µm, 1.4V**
  - Power (Watts)
  - Leakage: 0% 0% 1% 1% 2% 3% 5% 7% 9%
  - Active: 0% 0% 0% 0% 0% 0% 0% 0% 0%
  - Temp (C): 30 40 50 60 70 80 90 100 110

- **0.13µm, 1V**
  - Power (Watts)
  - Leakage: 1% 2% 3% 5% 8% 11% 15% 20% 26%
  - Active: 1% 2% 3% 5% 8% 11% 15% 20% 26%
  - Temp (C): 30 40 50 60 70 80 90 100 110

- **0.1µm, 0.7V**
  - Power (Watts)
  - Leakage: 6% 9% 14% 19% 26% 33% 41% 49% 56%
  - Active: 6% 9% 14% 19% 26% 33% 41% 49% 56%
  - Temp (C): 30 40 50 60 70 80 90 100 110
• Design issues:
  – Dynamic circuits may fail
  – Design workarounds needed to guarantee burn-in functionality

• Test issues:
  – IDDQ testing may become ineffective
  – Thermal-runaway problems, especially at burn-in
Conclusion

• We still have not found a fundamental barrier to extending Moore’s law

• The challenges are Power and Efficiency
  – Focus on dissipation, delivery, density

• VLSI technology scaling is expected to continue for the next decade